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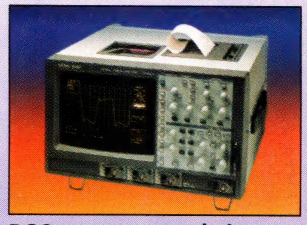
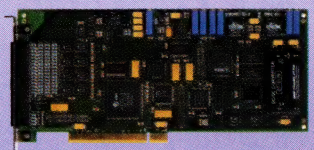
THE DESIGN MAGAZINE OF THE ELECTRONICS INDUSTRY

FEBRUARY 2, 1995





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1994 Finalists

pg 35

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Si9712DY	0.12Ω	0.15Ω	0.07Ω	0.06Ω	2 ms
Si9706DY	V_{CC} only		0.08Ω	0.07Ω	2 ms
Si9707DY	V_{CC} only		0.08Ω	0.07Ω	2 ms

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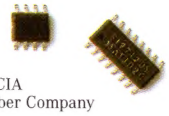

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• SBL-1X	10-1000	6.0	40	40	+7	6.25
SBL-1Z	10-1000	6.5	35	25	+7	7.25
SBL-1-1	0.1-400	5.5	35	40	+7	7.25
SBL-3	0.025-200	5.5	45	40	+7	7.25
• SBL-11	5-2000	7.0	35	30	+7	18.75
SBL-1LH	2-500	5.8	68	45	+10	5.50
SBL-1-1LH	0.2-400	5.2	64	52	+10	8.25
• SBL-1XLH	10-1000	6.0	40	55	+10	7.25
SBL-2LH	5-1000	5.9	61	54	+10	8.25
SBL-3LH	0.07-250	4.9	60	53	+10	8.25
• SBL-11LH	5-2000	7.0	45	30	+10	19.75
SBL-1MH	1-500	5.5	45	40	+13	9.80
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EDN Innovation 1994

EDN's Innovation Competition: The Biggest Field Ever! 35
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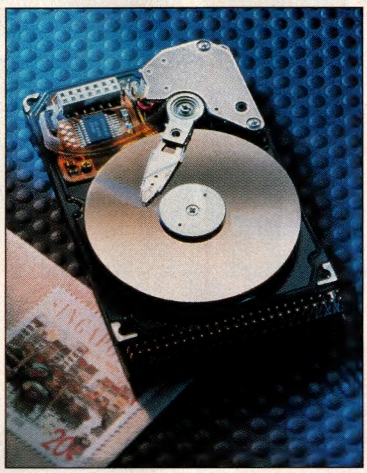
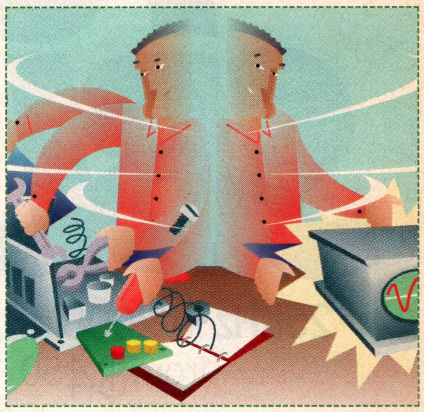


Miniature hard disks slip data and programs into your pocket 85



Try *fixing it* yourself 123

EDN

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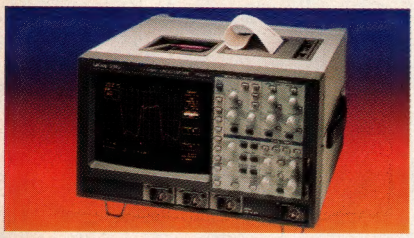

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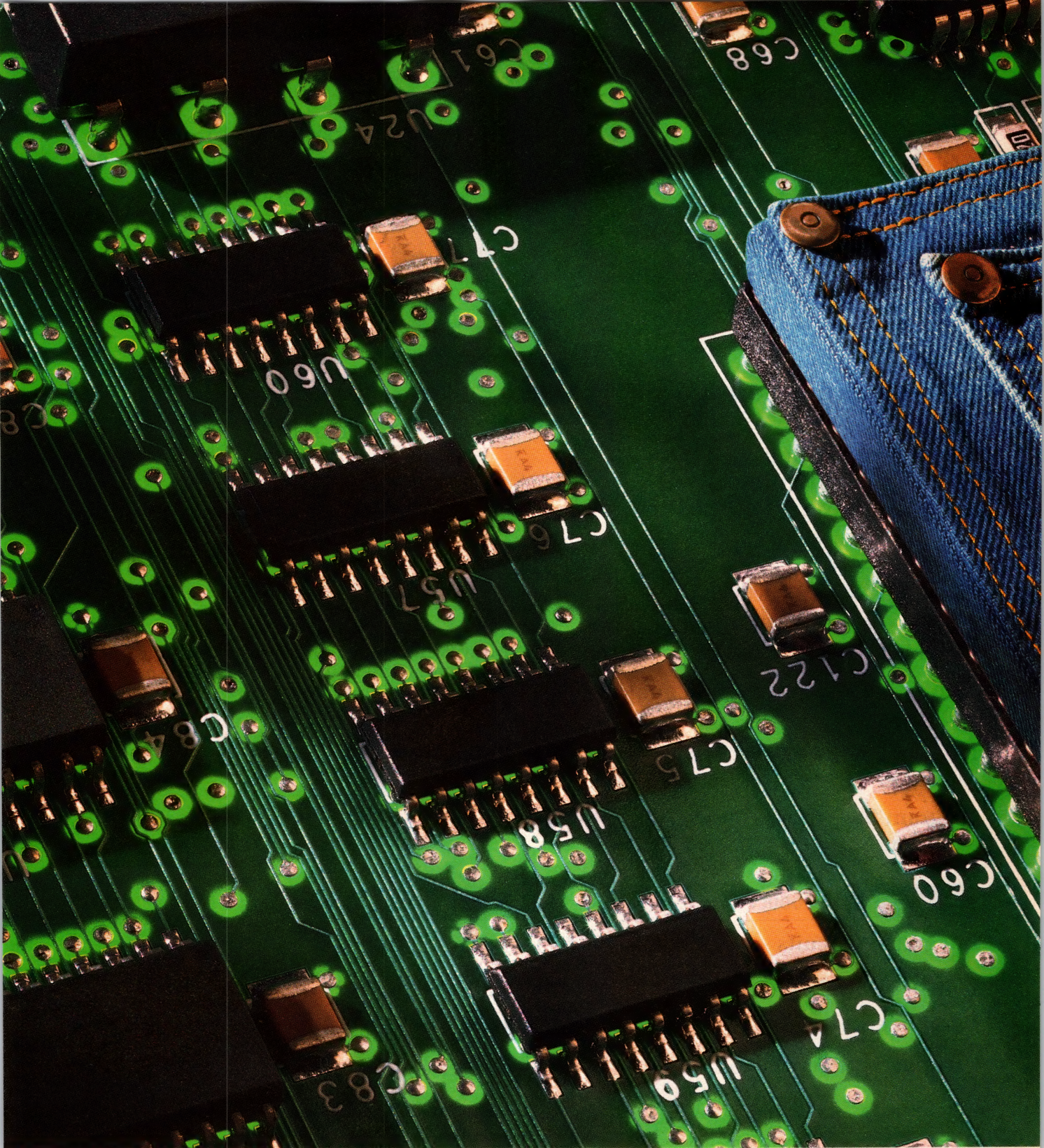

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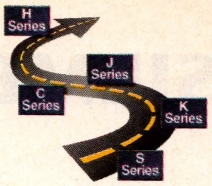

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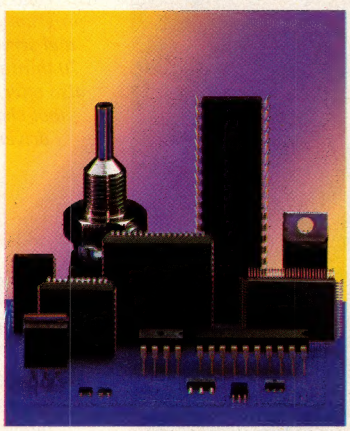
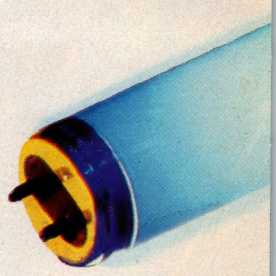


So as the number of applications for switched mode power supplies and motor controllers grows – and energy becomes more expensive – what better reason could there be for intelligent IC solutions?



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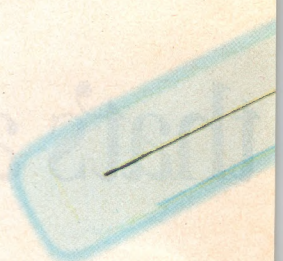

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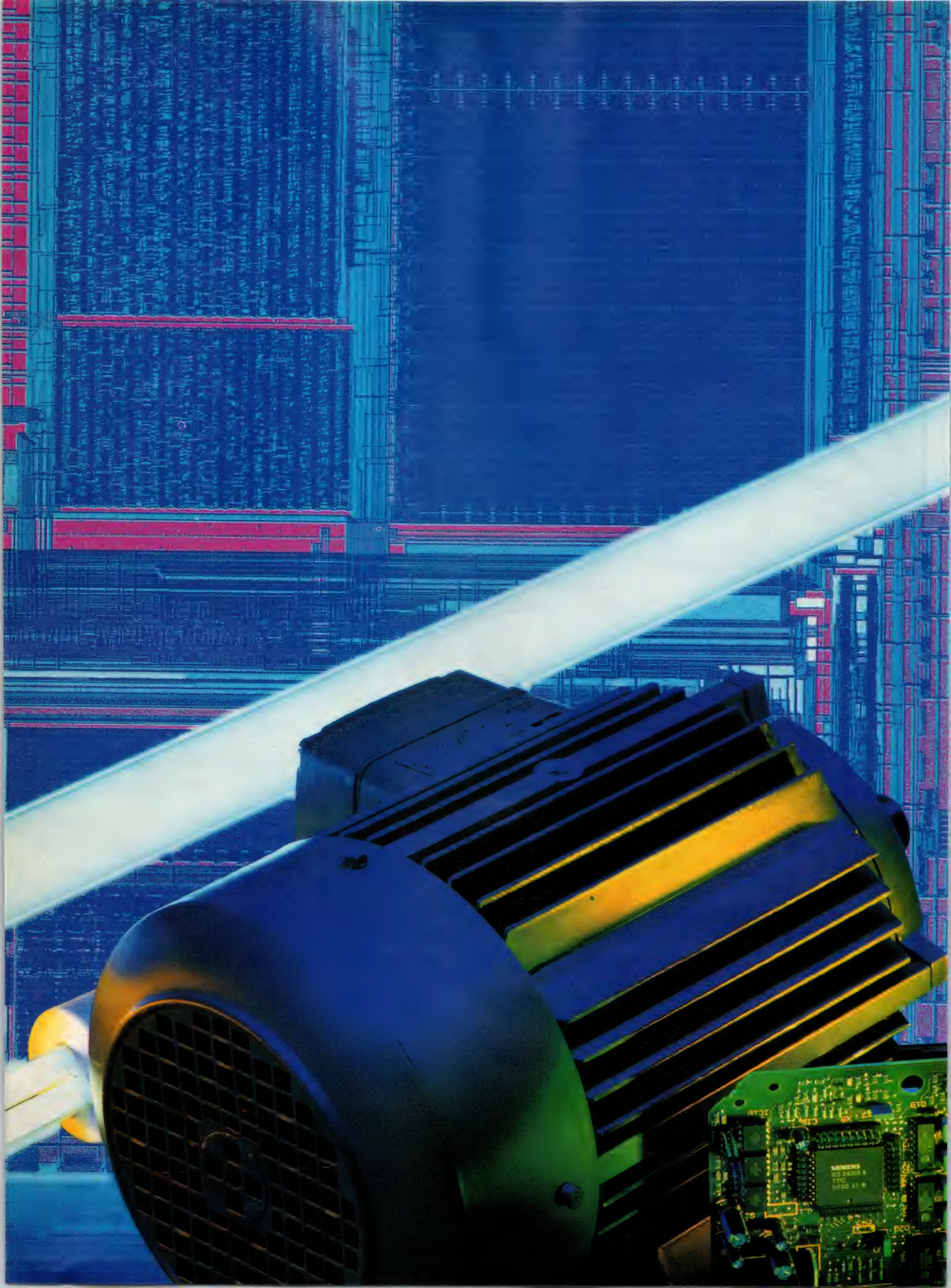

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CIRCLE NO. 162

DSO PUSHES REAL-TIME SAMPLING RATE TO 10G SAMPLES/SEC

SEVERAL TIMES A YEAR, a digital-scope vendor ratchets up the top real-time sampling rate available in such instruments. Since Hewlett-Packard's early-1993 introduction of the 54722A plug-in for the 54720D mainframe, however, the highest real-time sampling rate has held fast at 8G samples/sec. Now, at least for a while, LeCroy Corp has captured the real-time sampling-rate championship. In single-channel mode, the company's 9362 DSO takes 10G samples/sec. Even more impressive than its sampling rate are the scope's size and its price. At 22 lb, the 8.5×14.5×16.25-in. unit is decidedly portable, whereas the 54720D is an 8¾-in.-high unit for rack mounting or benchtop use. At $14,499, the 9362 costs roughly one-fourth as much as the 54722A/54720D.

In the 10G-sample/sec real-time-capture mode, the 9362's memory depth is only 1000 points, and its bandwidth is 750 MHz. The HP unit offers a memory depth of 128k points and a bandwidth of 2 GHz. The 9362 does offer deeper memory and higher bandwidth modes, however; when taking 100M samples/sec or fewer, the memory depth is 25k points. Also, for repetitive phenomena, the 9362 offers a random equivalent-time sampling mode. In that mode, the top effective sampling rate is 10G samples/sec on each of the unit's two channels, and the bandwidth doubles to 1.5 GHz. Among the 9362 options are a floppy-disk drive (standard on the HP unit), an internal graphic recorder for hard-copy output, and plug-in memory enhancement via either a PCMCIA RAM card or a PCMCIA hard disk. The HP unit does not offer the last three options. Another difference between the units is their displays: The 54720D features a color display; the 9362's display is amber monochrome.

You may wonder how LeCroy was able to pack this combination of features into a scope at this price. At the heart of the package is a patented 512-channel S/H chip that first appeared in the 5G-sample/sec 9360, which debuted 18 months ago. The S/H IC stores waveform samples until the ADC—a relatively inexpensive 100M-sample/sec, 8-bit flash device—can digitize them. In the 9362, two of the S/H chips capture interleaved samples, displaced in time by 100 psec.—by Dan Strassberg

Hewlett-Packard Co, Santa Clara, CA, (800) 452-4844. **Circle No. 487**

LeCroy Corp, Chestnut Ridge, NY, (800) 553-2769. **Circle No. 488**

The family resemblance between the 9362 and LeCroy's other two-channel scopes is striking. What you can't tell from the outside, though, is that, in single-channel mode, this unit offers the fastest real-time sampling of any DSO.

Publication guides engineers through the Internet. A new publication from Soliloquess Communications, *Science & Engineering Network News*, helps scientists and engineers ferret out Internet resources. Initially a monthly newsletter, the publication will soon have an accompanying on-line service. The service will focus on news, reviews, and tutorials of science and engineering resources on the Internet and related bulletin boards. It covers File Transfer Protocol and Telnet sites, electronic mailing lists, Usenet news groups, World Wide Web pages, frequently asked questions, and more. Charter subscription rate is $97/year; regular subscription rate is $195/year. Soliloquess Communications, Worcester, MA, (508) 755-5242. Circle No. 489

Data-acquisition boards are first on PCI

Data Translation has become the first vendor to offer PCI bus data-acquisition boards. According to rumors, all of the company's major competitors are working on such boards. In frame grabbers, the company is probably the third—rather than the first—to announce a PCI bus unit. However, its PCI frame grabber, the $995 DT3155, is significantly less expensive than the competitive offerings and provides better resolution in monochrome applications. (According to Data Translation, all of the boards promise 8-bit resolution, but the competitive ones deliver less.) Data Translation achieves the board's attractive performance and price by eliminating the

(Continued on pg 12)

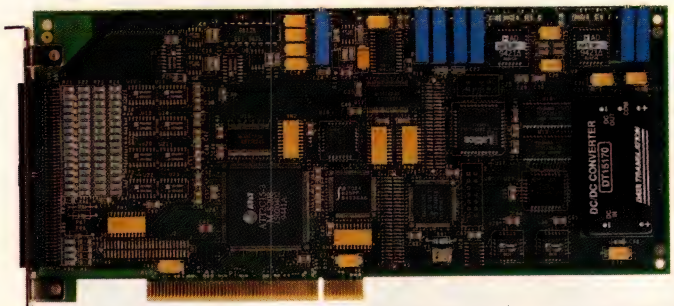
video chip set; such chip sets are optimized for color performance, but using them also increases a board's cost and degrades its monochrome performance.

The three data-acquisition boards include the $995 DT3001 with 16 single-ended and eight differential inputs, the $1095 DT3002 (32/16 inputs), and the $1395 DT3003 (64/32 inputs). All three boards take 330k 12-bit samples/sec in the single-channel mode, and all offer eight digital I/O points. In multichannel mode, the DT3001 takes 250k samples/sec, whereas the other two models each take 100k samples/sec. The DT3001 and DT3003 each offer a pair of 12-bit analog outputs. Boards designed to revision 2.0 or higher of the PCI spec provide true Plug-and-Play operation under Windows 95 and are compatible not only with PCs but also with workstations based on a variety of μPs. The boards do not need DMA or massive amounts of RAM. PCI data-acquisition boards send data directly to the host computer's motherboard RAM.

—by Dan Strassberg

***Data Translation Inc**, Marlborough, MA, (508) 481-3700.*

Circle No. 490



One of the advantages of PCI for data acquisition is that it does away with the need for significant onboard RAM, which makes possible smaller, simpler boards.

Second-generation DECT baseband processors save power

The Digital European Cordless Telephone (DECT) standard has been in place for around two years, and vendors are moving on to second-generation silicon with higher integration and lower power. SiTel Sierra's CMOS, 80-pin QFP SC14401 and SC14420 baseband processors exemplify this move and require only a microcontroller and RF front end to complete the electronics for a base station or a handset that works for 10 hours in operation or 100 hours in standby mode.

The SC14401 ($9.90) for handset and base-station applications handles one trunk line and three DECT channels. The SC14420 ($12.90) suits domestic-base-station applications and handles two trunk lines and six DECT channels. Both processors operate on 3.3 to 5V, and the SC14401 consumes less than 8 mA in duplex voice mode and less than 1.2 mA in paging mode. Both processors include a 14-bit, linear, second-order, sigma-delta coder-decoder; an adaptive-differential-pulse-code-modulation (ADPCM) transcoder; burst-mode logic; a scrambler/descrambler; an encryptor/decryptor; and character-recognition check logic. The processors also include a Gaussian filter (BT=0.5) and programmable amplitude control (eight steps/dB) for direct modulation output.

The SC14420 has an additional ADPCM transcoder to enable two full-duplex channels and a 2-kbyte memory with linear addressing for six speech channels.

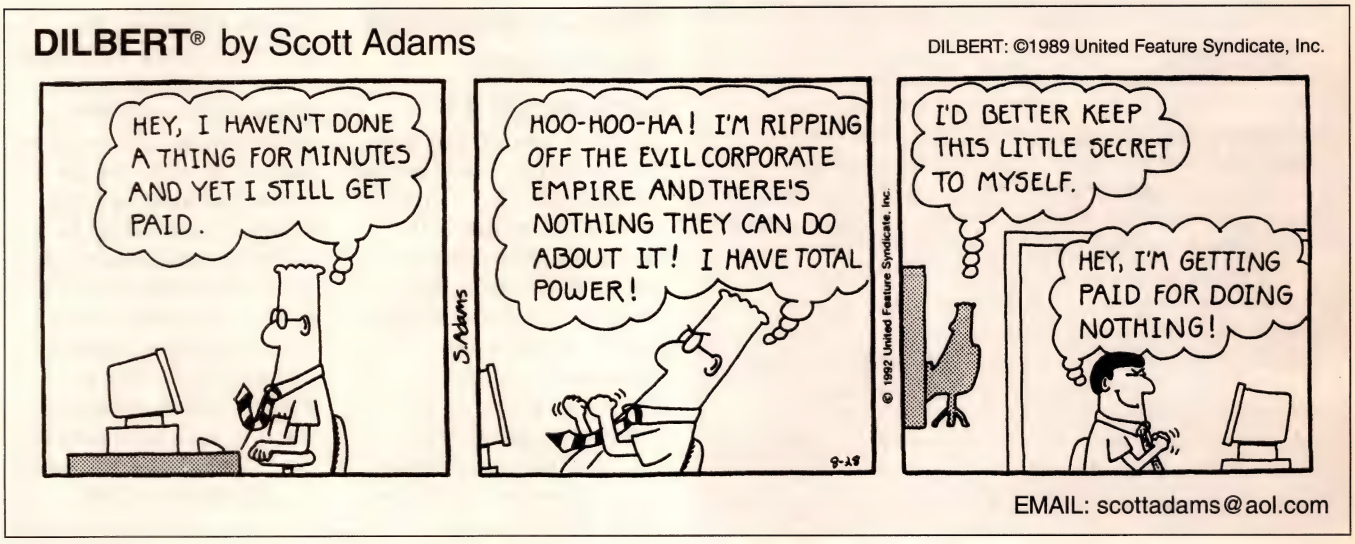
—by Brian Kerridge

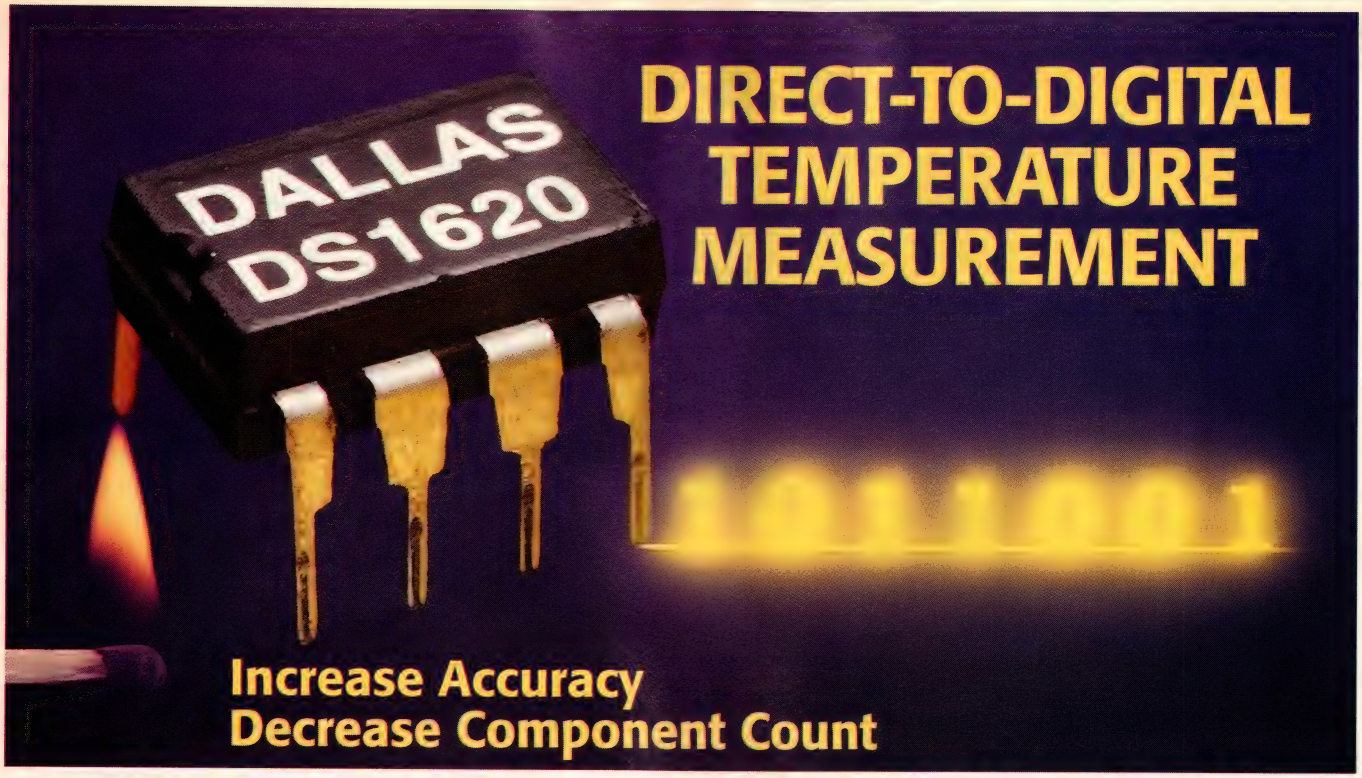
SiTel Sierra, 's-Hertogenbosch, The Netherlands. (31) 73 40 88 22. **Circle No. 491**

Universal programmer verifies at 3.3V

ICE Technology's Micromaster LV programmer includes separate 3.3 and 5V circuitry to verify devices in each voltage range. Typically, programmers rely on 5V circuitry to verify 3.3V devices, and, in practice, this method can

(Continued on pg 14)





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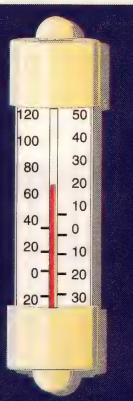

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CIRCLE NO. 88

stress internal protection diodes or produce misleading errors due to input thresholds.

The Micromaster LV programs more than 90 microcontrollers and a wide range of EPROMs, EEPROMs, flash, and other PLDs. You can extend the range to devices with more than 40 pins by using optional adapters. The programmer uses device vendors' algorithms, including quick programming versions; for example, you can program a Microchip PIC16C54 in 500 msec. AMD, Atmel, Microchip and National Semiconductor have given vendor approval for the programmer.

ICE Technology's Micromaster LV universal programmer verifies 3.3V devices under actual operating conditions and emulates up to 512×16-bit RAM/ROMs.

PC software operates under MS DOS or MS Windows, and the programmer links directly to a PC's parallel port. Software updates to include new devices are free via bulletin-board system ((44) 1226 761181). Standard software also allows you to test SRAMs and DRAMs.

By adding optional cards, you can also convert the programmer to an 8- or 16-bit RAM/ROM emulator. The unit emulates 3.3 and 5V devices, with up to 512×8- or 16-bit organization. The emulator includes bidirectional communications, a target-system reset, and the ability to alter memory on the fly.

The programmer operates from an external line adapter/charger or internal batteries for field use. Programmer, software, charger, and cable cost $999.

—by Brian Kerridge

ICE Technology, Penistone, UK. (44) 1226 767404.
Circle No. 492

Floating-point DSP breaks $10 barrier

A 32-bit, floating-point DSP costing less than $10 has arrived: the TMS320C32 from Texas Instruments. This breakthrough allows designers of DSP applications to take advantage of the performance and ease of use of a floating-point processor. Besides an already present variety of algorithms for the floating-point architecture, the register-based C32 has rich addressing modes and software-stack support, making it suitable for developing algorithms using C programming. Typically, programmers prefer developing DSP algorithms using floating-point math because it is much less complicated and cumbersome than fixed-point math. But, because floating-point DSPs were too expensive for many applications, software programmers had to convert their floating-point algorithms to run on less expensive fixed-point DSPs.

The C32 also offers several other beneficial features. It is object-code-compatible with TI's previous generation C30/C31 DSPs, allowing programmers to use previously written algorithms on the C32. The device integrates a 64-word program cache, two 32-bit timers, a synchronous serial port, two lower power modes, and a two-channel DMA coprocessor. It also stores multiplication results in a 40-bit register file comprising a 32-bit mantissa and an 8-bit exponent.

From a system perspective, the C32, which comes in a 144-pin PQFP, has a flexible memory interface, allowing connection to 8-, 16-, and 32-bit-wide memories. You can even mix and match memory configurations within the same system, letting you make essential trade-offs between system cost and performance.

New third-party products supporting the C32 include evaluation/target boards from DSP Research (Sunnyvale, CA) and Loughborough Sound Images Ltd (Loughborough, UK). These products include debugger and C-compiler support. They also handle all I/O communications between I/O devices on the DSP board and the PC host.

TI is planning to begin sampling the TMS320C32 this quarter and will offer 40-, 50-, and 60-MHz versions. Price is $9.95 (250,000).

—by Markus Levy

Texas Instruments Literature Response Center, Denver, CO, (800) 477-8924, ext 4500.
Circle No. 493

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t_{on}	400 ns max	1000 ns max	1000 ns max
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I_{DD}	0.2 mA max	2.0 mA max	2.0 mA max

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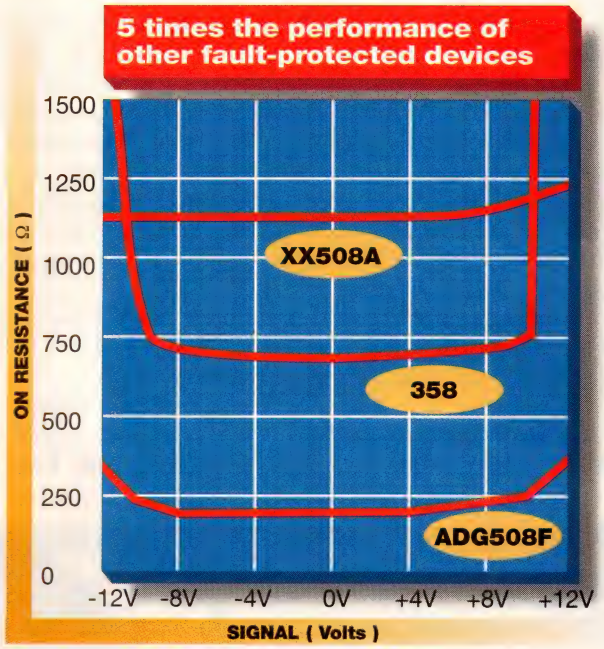

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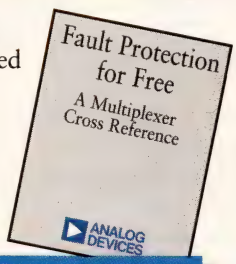

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CIRCLE NO. 157

TMS320C44 DSP modules feature 8-Mbyte SRAM

The single-processor MDC44S and dual-processor MDC44T DSP modules from Loughborough Sound Images are the first of a series based on the Texas Instruments 50-MHz TMS320C44 processor. Using a 4.2×2.5-in. TIM-40 standard plug-in card, the modules are compatible with the company's VMEbus and PC-carrier boards.

Each module uses the plastic-packaged TMS32C44 for increased memory capacity of up to 8 Mbytes of zero-wait-state SRAM. Memory comprises four banks of 28k×32- or 512k×32-bit, zero-wait-state SRAM split equally between the TMS320C44's local and global buses.

The dual-processor MDC44T offers as much as 4 Mbytes of SRAM per processor and includes a 32k×8-bit, programmable, erasable ROM on the local bus for nonvolatile storage, or for booting up when the device runs independently of a host.

Both module interfaces also include six 20-Mbyte/sec, 8-bit parallel ports. Prices for the MDC44S and MDC44T start at $2700 and $5200, respectively.

—by Brian Kerridge

Loughborough Sound Images, Loughborough, UK. (44) 1509 634444. **Circle No. 494**

High-performance ATM data transmits via HIPPI

GTE Government Systems has announced the first successful transmission of high-performance supercomputing data streams using an asynchronous-transfer-mode (ATM) switch with a built-in high-performance, parallel-interface (HIPPI) module. The HIPPI module plugs directly into an ATM switch.

Using GTE's Secure Prioritized ATM network (SPANet) switch, the HIPPI module encapsulates the data into ATM cells using ATM Adaptation Layer type-5 and routes the data from a Cray EL94 supercomputer back to its network destination. The ATM cells then convert back to HIPPI-formatted data streams and transmit to a remote PsiTech frame buffer.

The GTE HIPPI module operates in full-duplex mode when source and destination processing occur simultaneously and independently. Users can select data rates from 30 to 100 Mbps in 10-Mbps increments. The GTE module lets users extend HIPPI circuits to thousands of miles by creating ATM cells that carry HIPPI-formatted data from one supercomputer to another across a wide-area ATM network. Previously, extending HIPPI circuits required serial-HIPPI extension equipment.

—by Fran Granville

GTE Government Systems Corp, Needham Heights, MA, (617) 455-5152. **Circle No. 495**

Philips and Sony propose multimedia-CD specs

Philips Electronics and Sony Corp have jointly proposed specifications for a 12-cm-diameter, high-density, multimedia CD. The two companies hope the specifications, which will emerge in final version by midyear, will become the basis for future optical media. The specifications include the ability to store 3.7 Gbytes of data—more than five times that of current CDs. The disks achieve this capacity by incorporating a 635-nm (red) laser, reducing both the distances between the tracks and the sizes of the pits, and by using sophisticated error-correction and improved modulation techniques.

The specifications would allow manufacturers to produce the disks at conventional manufacturing facilities with only minor modifications. As a result, production costs will be similar to those of conventional CDs, according to the companies.

The specification also includes a dual-layer version, which doubles capacity to approximately 7.4 Gbytes. The companies are working with 3M Co to develop the technology for this version. A possible application for the disks would be a "digital video disk" that would provide 135 minutes of MPEG-2-quality video and multitracks of compressed digital audio and subtitling. The use of a variable 1- to 10-Mbps transfer rate for video would allow higher picture quality than that of current consumer video systems. Other applications include interactive entertainment, games, and ultra-high-quality-sound audio.

A group of experts from Apple Computer Inc, Compaq Computer Corp, IBM Corp, and Microsoft Corp is discussing how the high-density CD-ROM could support existing CD-ROM applications. They are considering extensions of the volume and file standard to accommodate the high-density devices, based on the physical specifications of the disks. The group is also recommending the adoption of the ISO 9660-standard CD-ROM file structure with suitable extensions for use as the data-interchange platform between existing and high-density CDs.

—by Fran Granville

Philips Electronics, Los Angeles, CA, (310) 444-6175. **Circle No. 496**

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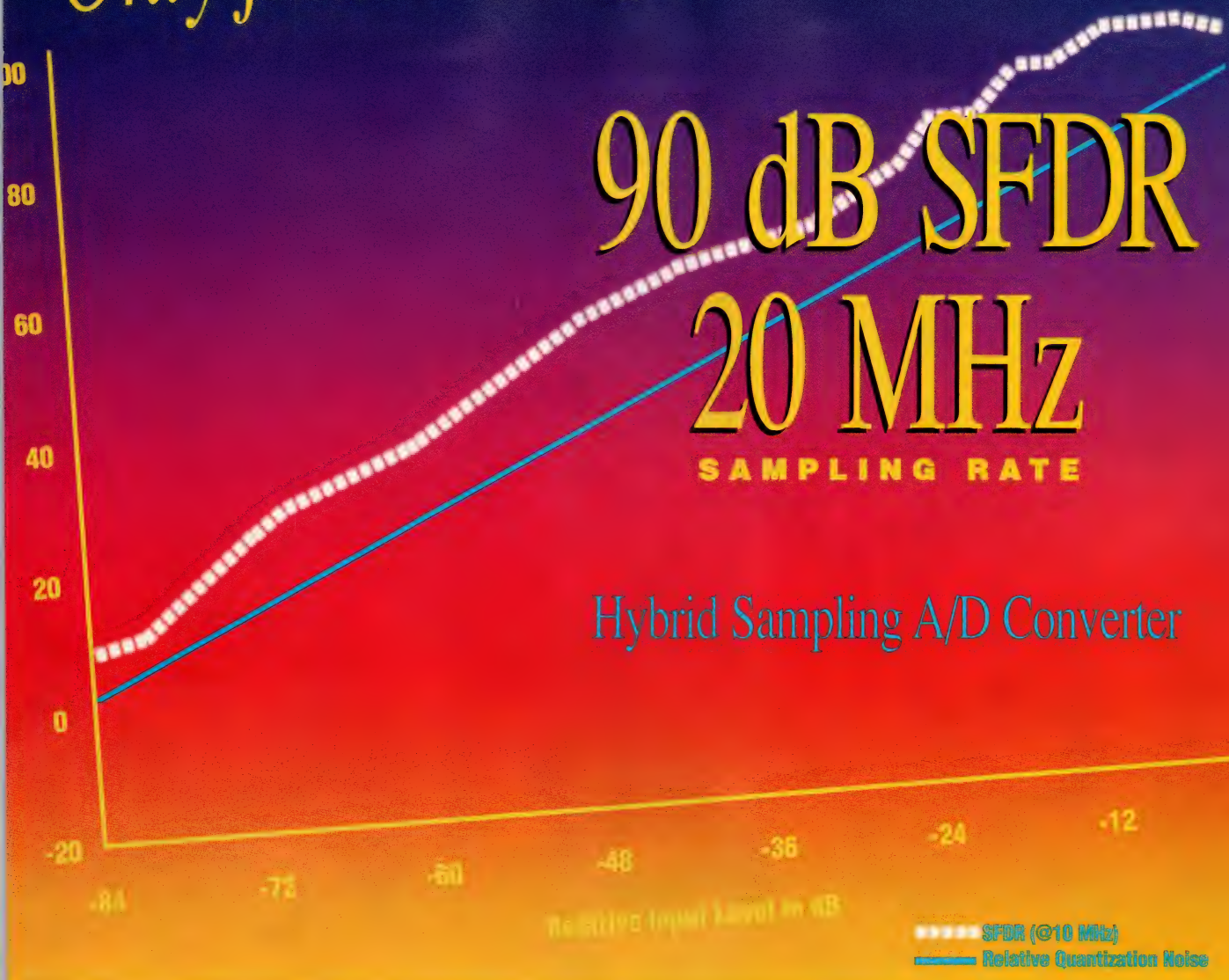

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		GVGC450/453	GVGC650/650L	GVSC450	GVS470	GVSC653	GVSC670
Process		0.8 micron CMOS	0.6 micron CMOS	0.8 micron CMOS	0.8 micron CMOS	0.6 micron CMOS	0.6 micron CMOS
Metal		2LM/3LM	2LM/3LM	2LM	2LM	2LM/3LM	2LM
Usable Gate		2LM:4K to 133K 3LM:7K to 232K	2LM:13K to 260K 3LM:22K to 500K	up to 300K	up to 350K	up to 780K	up to 1,110K
Pad Count		80 to 434	104 to 524	up to 444	up to 444	up to 524	up to 524
Number Of Base Array		16	24	–	–	–	–
Operating Voltage		5V	3.3V/5V	3.3V/5V		3.3V/5V	
Gate Delay (Fan out=2)		205PS	5V : 130PS 3.3V : 180 PS	190 PS	195 PS	5V : 160 PS 3.3V : 220 PS	5V : 193 PS 3.3V : 266 PS
Toggle Freq.		360 MHz	690 MHz	340 MHz	330 MHz	640 MHz	490 MHz
Power Consumption		3.7μW/gate/MHz	5V:3.6μW/gate/MHz 3.3V:1.3μW/gate/MHz	3.4μW/gate/MHz	1.9μW/gate/MHz	2.7μW/gate/MHz	0.6μW/gate/MHz
Output Drive (mA)		2,4,8 or 12	2,4,8,12 or 24	2,4,8,12 or 24		2,4,8,12 or 24	
ROM	Max.bit Size	32K	128K	128K		128K	
RAM	Max.bit Size	64K	128K	128K		128K	

*0.5 micron will be available from the 2nd quarter of 1995.

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Revisiting Decade 90: Design for Test

In early 1988, I wrote a five-part series called "Decade 90: The future of system design." In it, I tried to forecast the major technological trends that would shape our industry in the 1990s. This is the third in a series of five mid-decade editorials looking at how close the predictions came.

You could probably say that system designers don't like design for test (DFT) any better in 1995 than they did in 1988, for the same reasons. DFT techniques take extra time, slap a performance penalty on the design, and eat up precious silicon that could be used to provide other features. Nevertheless, designers **are** using DFT techniques more now than in 1988. For example, about 60% of LSI Logic's ASIC design starts now incorporate boundary scan. With big ASIC designs, DFT may be the only way to make the initial design verification of a working 100,000-gate ASIC; the ability to test the ASIC in manufacturing is gravy.

Back in 1988, it was becoming clear that board-level manufacturing technologies such as surface-mount technology (SMT) made bed-of-nails board testing nearly impossible. Today, we build almost everything using SMT, and multichip modules are delivering still smaller, even more untestable geometries.

In 1988, Paul Gifford, manager of central systems engineering at Sequent Computers, estimated that the DFT performance penalty was 5 or 6%. It's even lower now, but, for some designs, any speed penalty was and is unacceptable. Some things don't change over time. However, with several million transistors available on large chips, a few thousand dedicated to test don't seem onerous.

The Joint Test Action Group (JTAG) was already creating the serial-test standard in 1988. It now exists as the IEEE-1149 Standard, and many semiconductor vendors have pressed it into service for other features, such as device programming. Although you can now get many standard ICs and ASIC macros with JTAG ports, its use is still far from widespread.

One test technique, I_{DDQ}, didn't appear in the 1988 Decade 90 article, but it now has a growing number or proponents. One major reason for its growing popularity is that it's an after-the-fact test. Feed the chip a few carefully selected test vectors, watch how its current consumption jumps, and mark it faulty if its current consumption doesn't jump to the right tune. You don't have to use DFT if you use I_{DDQ}, a feature sure to win the hearts of harried system designers.

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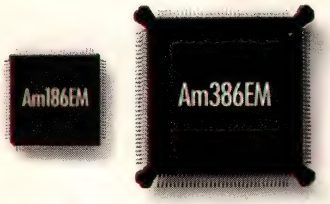

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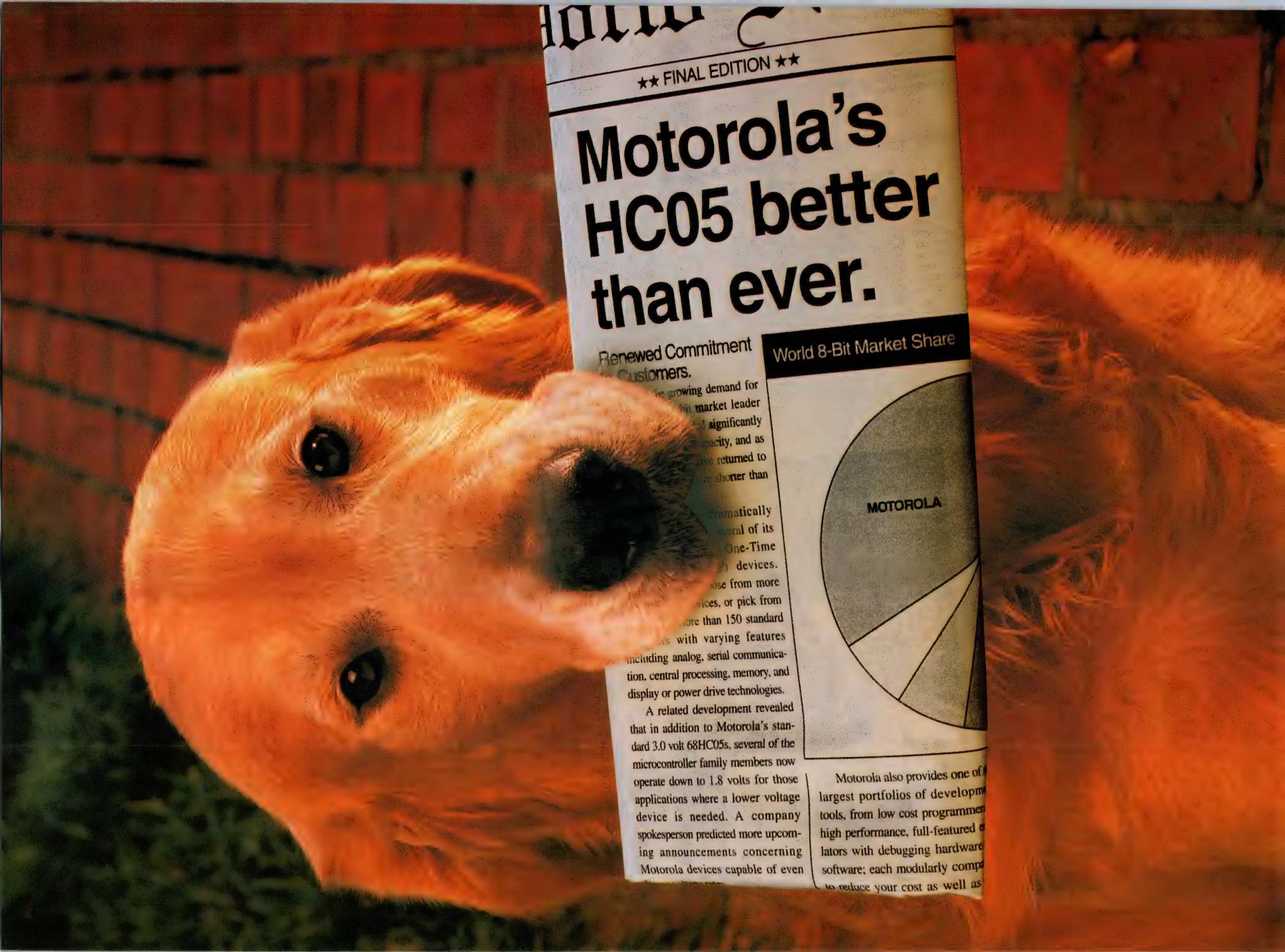
Insight
THE BEST IN THESE PARTS

CIRCLE NO. 94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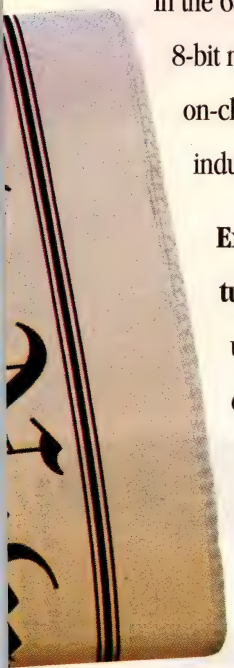
Who says there's no good news anymore?

Have you read the latest? If not, you'd better catch the news about Motorola's 68HC05 microcontroller family before you design another 8-bit solution.



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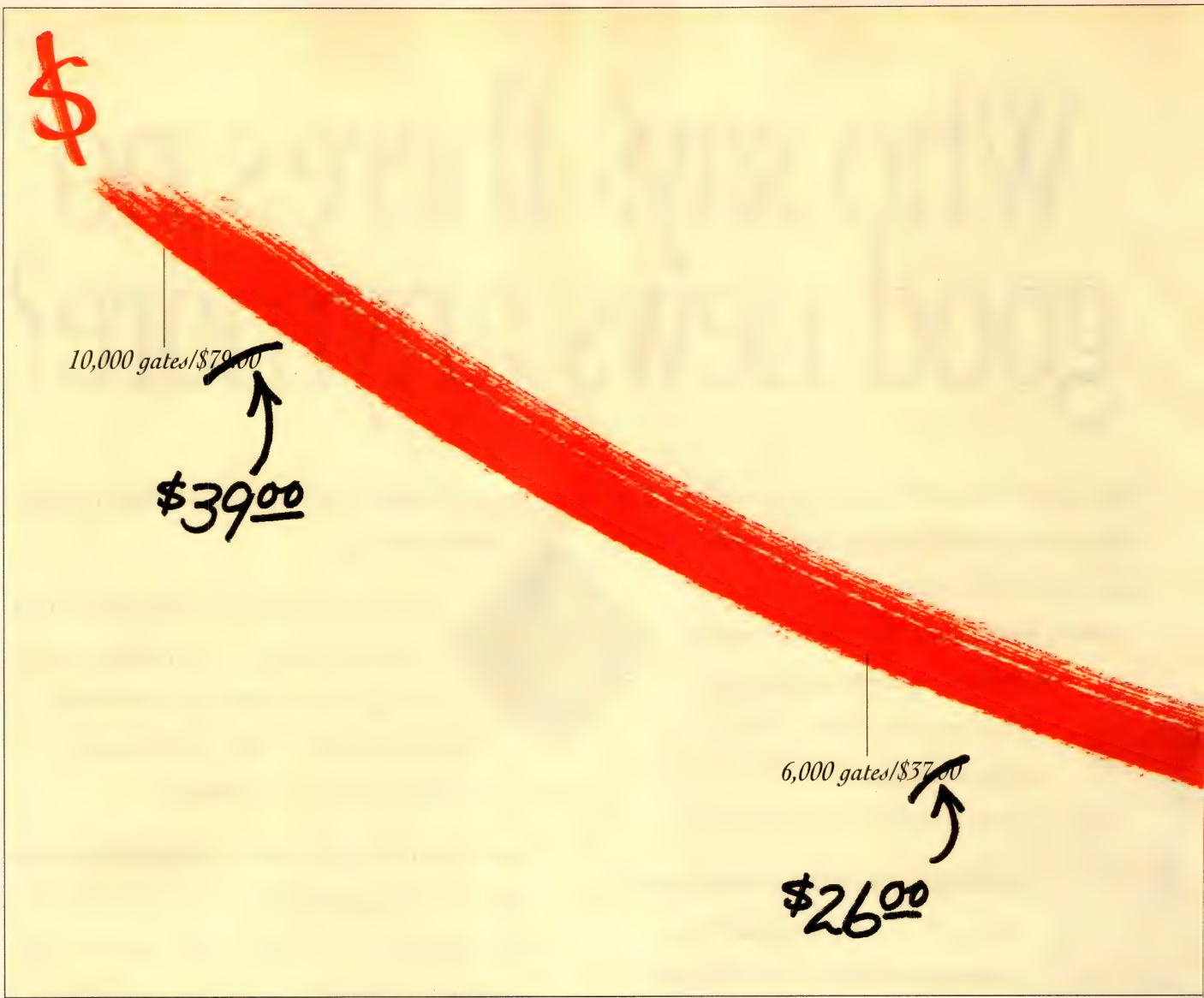
CSIC Microcontroller Division



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And really, it was no trouble at all. We simply reduced the price of *our* product—Xilinx™ FPGAs.

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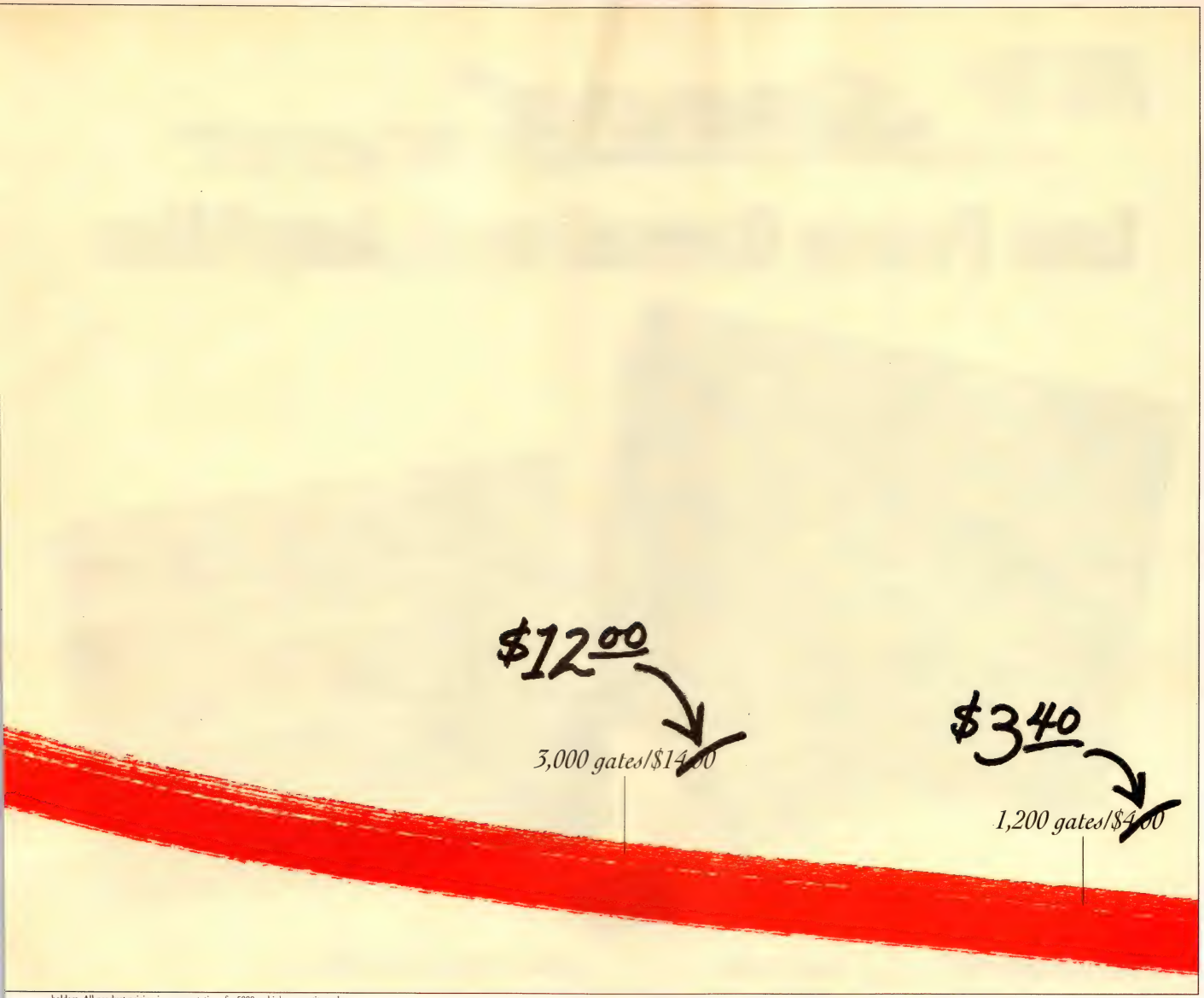

holders. All product pricing is representative of a 5000 or higher quantity order.

But the impact doesn't stop with your product. What we've done, in effect, is serve notice on the gate array market. To whom we say the following: objects in mirror are closer than they appear.

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CIRCLE NO. 155

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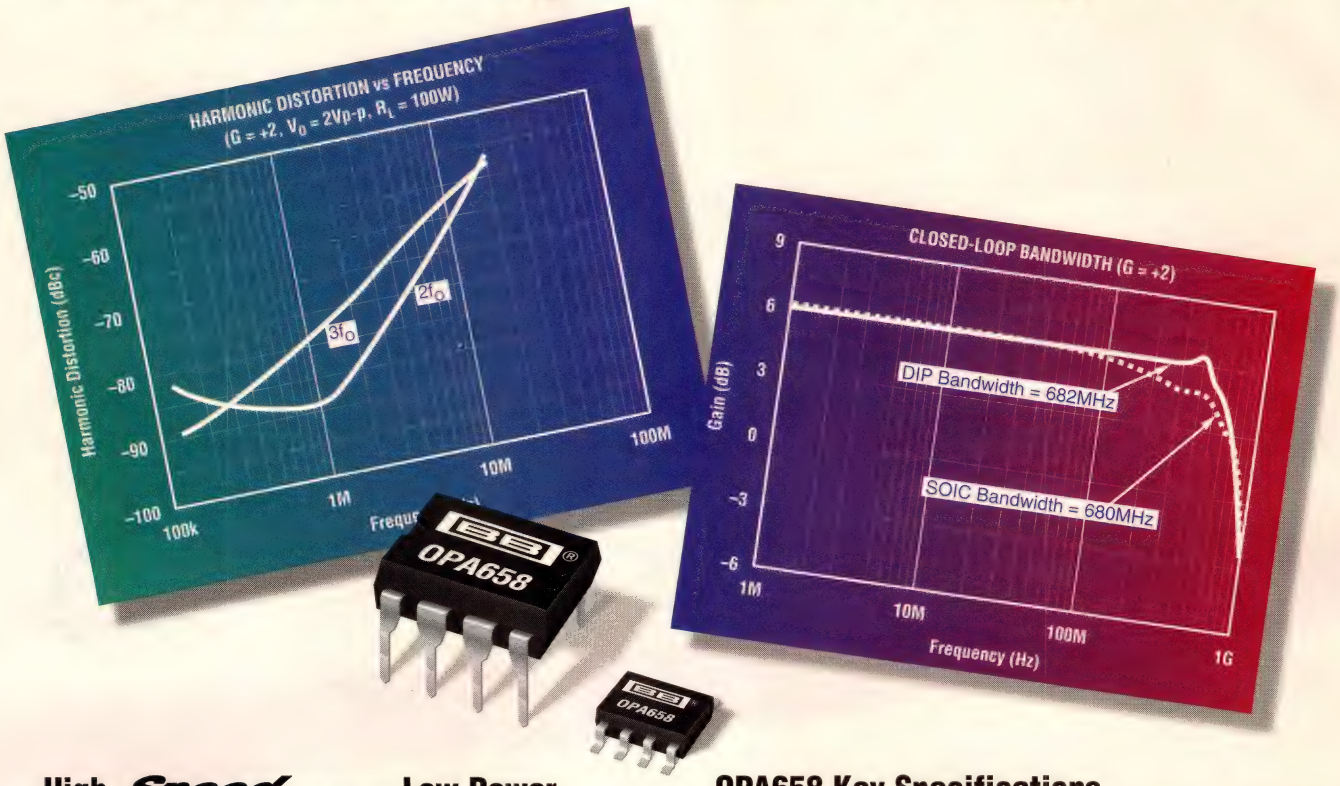

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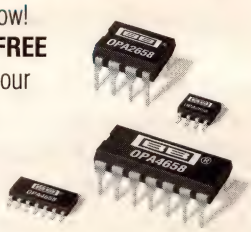

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CIRCLE NO. 159

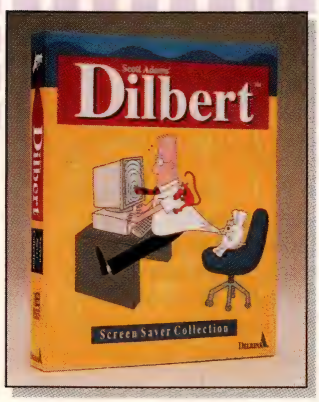
EDN's Innovation Competition:
THE BIGGEST FIELD EVER!

Vote for innovation, and enter to win a Dilbert screensaver. This is Year Five for *EDN*'s Innovation and Innovator of the Year Awards competition, and the field is bigger and, frankly, better than ever. Since 1990, we have paid tribute to the innovative products and people in the electronics industry by asking our readers to vote on finalists selected by *EDN*'s editors from a field of nominations. This year, we received more high-quality entries than ever before.

Innovation

Our job—selecting finalists—was really tough. Your job is even tougher. Please read and carefully consider the entries in each of the nine categories for the most innovative products and people of 1994. Vote on the postage-paid ballot card that appears in this special Innovation Award section. An independent research company will tally your votes, and we'll announce the winners in our April 13, 1995, issue.

Be sure to mail your entry ballot. We'll hold a random drawing from the Innovation Award ballots, and 10 lucky voters will win copies of the new Dilbert Screensaver Collection for Windows from Delrina Corp. You already know "Dilbert," the popular engineering-oriented comic strip by Scott Adams. *EDN* started running "Dilbert" last year, and your response has been wildly enthusiastic. The Dilbert Screensaver Collection more than satisfies your minimum daily humor requirement with a regular dose of Dilbert, Dogbert, and Ratbert through pictures, animation, and sound. So please vote now, and help *EDN* celebrate innovation.

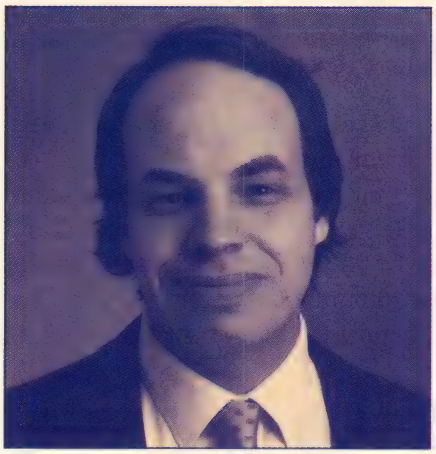


Vote in *EDN*'s Fifth Annual Innovation of the Year Awards, and you might win one of 10 copies of the Dilbert Screensaver Collection for Windows from Delrina Corp (San Jose, CA, (800) 268-6082). Dilbert characters: © 1989 UFS Inc.

EDN

Innovation 1994

INNOVATORS



ROBERT W ADAMS

After a brief career as a professional musician, Bob Adams decided to dedicate his expertise and his engineering degree to audio electronics. In 1977, he joined dBx Inc and designed oversampling A/D converters for digital audio equipment. He became the Director of Research at dBx, and his work led to an early recording system that employed companded delta modulation and a 20-bit sigma-delta A/D converter. He joined Analog Devices in 1989 to manage a design team for digital audio converters and was recently promoted to Manager of Audio Technology. His work produced the AD1879, the industry's first sigma-delta A/D converter with true 18-bit performance. Most recently, Adams designed the AD1890 asynchronous sample-rate converter, which can convert audio bit streams of one rate to that of any other. The $28.90 (1000) AD1890 performs the same functions previously performed by DSP-based board and box products costing $1000 to $10,000.

The AD1890 uses a sample-rate conversion technique called polyphase filtering. This technique employs an oversampled FIR lowpass filter with thousands of times the number of coefficient samples required to meet the Nyquist criterion. This technique avoids the need to run the oversampling filter at thousands of times the maximum input signal frequency. The AD1890 has on-chip filter coefficients representing the equivalent of 65,536 polyphase filters. Each filter processes the 64 most recent samples with a fractionally different group delay. The net result is to achieve extremely high oversampling rates while keeping on-chip operating frequencies in the megahertz range. Since its introduction, the AD1890 has appeared in digital mixing consoles, recordable-CD equipment, digital-audio workstations, studio-to-transmitter links, and stand-alone sample-rate conversion equipment. Adams holds nine patents and has published 16 papers on electronics and audio topics.

To vote for this entrant as Innovator of the Year, mark the appropriate box on the ballot.

ANALOG DEVICES INC
NORWOOD, MA
(617) 329-4700

PAUL BASEHORE

Paul Basehore designed the NLX220 fuzzy-logic controller, implemented the ASIC realization of the IC, managed the team that created the chip's software development tools, and developed end applications for the µC. The NLX220 is a one-chip, stand-alone processor that employs fuzzy-logic techniques. It supports six different types of membership functions and implements floating membership functions that allow the center and width of any membership function to float dynamically, based on the incoming data. Although the signal processing is digital inside the NLX220, the µC brings signals on chip through four analog inputs feeding an 8-bit A/D converter. Its output stage consists of an 8-bit D/A converter and four sample-and-hold buffers for analog output. Thus, designers can drop this inherently digital processor into an analog signal path. The one-time-programmable version of the device costs less than $2 (1,000,000).

The NLX220 can perform first-, second-, and third-order derivative control functions, automatic calibration, and rule-based timing. The controller processes signals according to as many as 50 "rules" stored in its 256-byte EEPROM. Fuzzy-logic processing at a decision rate of 500,000 rules/sec allows the NLX220 to perform first-, second-, and third-order derivative control; automatic calibration; and rule-based timing at 10,000 samples/sec for each of the four analog channels. Because you program the device using fuzzy-logic rules instead of an algorithmic programming language, you can stay focused on your application rather than on writing code. Basehore has five patents related to fuzzy-logic and neural processing techniques and has written six papers on fuzzy logic for various international conferences.

To vote for this entrant as Innovator of the Year, mark the appropriate box on the ballot.

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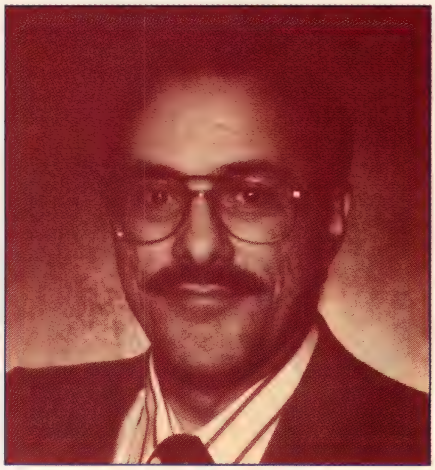

GERALD M COTREAU

Gerald Cotreau developed Harris Semiconductor's HC5506 dual SLIC (subscriber-line interface circuit) IC. This device is the first to implement two SLICs on one IC. It integrates the ring-relay function (thus eliminating the need for electromechanical components on the line card), eliminates the need for precision power resistors, permits the exclusive use of surface-mount components on the line card, and maintains the same performance and audio quality of existing state-of-the-art SLICs. Cotreau eliminated the need for a ring relay by placing the SLIC's driver-amplifier outputs in a high-impedance state during ringing. No physical switch exists, which reduces distortion. Cotreau also had to design output stages that could withstand a ring voltage of several hundred volts and a zero-current detector that shuts the amps off when ring current is present.

Cotreau also reduced the SLIC's operating power by 50%, so that he could put two of them in one IC package. He designed a current-mode SLIC that reads line voltages through current-sensing resistors, as do some other SLICs. However, the HC5506 processes

all signals in current mode. This approach allowed Cotreau to shift the SLIC's signal-processing circuitry from the 50V subscriber-line power to the 5V logic supply. This approach dropped the SLIC's idling power to 90 mW.

To vote for this entrant as Innovator of the Year, mark the appropriate box on the ballot.

HARRIS SEMICONDUCTOR
MELBOURNE, FL
(407) 724-7862

ROBERT C DOBKIN

Robert Dobkin is responsible for the design of a large number of the industry's standard analog ICs, including voltage regulators, amplifiers, comparators, and voltage references. He developed the industry's most stable monolithic reference and originated three-terminal adjustable voltage regulators, low-dropout linear regulators, silicon temperature sensors, and a monolithic replacement for optoisolators. Recently, Dobkin conceived and directed the development of the LT1585 voltage-regulator family, specifically designed for the needs of 3V, 32- and 64-bit μPs. These processors can require a 10A current step from the power supply when going from sleep to operating mode. The transition takes but nanoseconds, and the power-supply voltage must stay within narrow limits during the step. A regulator that can provide this sort of current step while operating with only 2V of "headroom" required twice the regulation-loop full-load response speed. Dobkin foresaw the need for this device, developed a technical solution, staffed a development team, and produced a working device just as the processors that required it appeared.

Currently, Dobkin heads a staff of more than 75 people at Linear Technology who are engaged in the design of high-performance bipolar, CMOS, and BiCMOS ICs. He directs all new-product development and internal applications support. He co-founded Linear Technology in 1981. During the 10 preceding years, he was the Director of Advanced Linear Circuit Design at National Semiconductor. Dobkin started his career as an analog designer at Philbrick Researches after attending MIT. Dobkin holds more than 35 patents and has authored more than 50 articles.

To vote for this entrant as Innovator of the Year, mark the appropriate box on the ballot.

LINEAR TECHNOLOGY CORP
MILPITAS, CA
(408) 432-1900

ERIC ETHERIDGE AND GORDON SHANK

Eric Etheridge and Gordon Shank developed the critical hardware and software components that allow the Tektronix 1-GHz, 4G-sample/sec TDS784A digitizing storage oscilloscope (DSO) to capture 400,000 waveforms/sec. This acquisition rate is faster than the world's fastest analog scopes, the Tektronix 7104 and 2467B, and is far faster than other DSOs, which spend less than 0.007% of their operating time acquiring data—usually capturing no more than a few hundred waveforms/sec. The TDS784A's fast-acquisition mode is called InstaVu.

The key to InstaVu's speed is a new 360,000-transistor demultiplexer IC developed by Etheridge. The IC's high-speed demultiplexer feeds the incoming 1-Gbyte/sec digitized-data stream from the DSO's A/D converter into a 64-bit-wide acquisition-and-display memory. The IC also incorporates a 9-MIPS DSP and rasterizer circuits. The DSO contains four of these demultiplexer ICs, one for each channel. Equally important are the distributed software algorithms developed by Shank, which team the TDS784A's several μPs: a Motorola 68020, a Tektronix TriStar DSP, and the DSPs in each of the DSO's four demultiplexer chips.

To vote for this entrant as Innovator of the Year, mark the appropriate box on the ballot.

TEKTRONIX INC
MEASUREMENT BUSINESS DIV
BEAVERTON, OR
(503) 627-1807

VXIPLUG & PLAY SYSTEMS ALLIANCE FOUNDING MEMBERS

On September 22, 1993, at the AutoTestCon show in San Antonio, TX, a small group of VXI product vendors announced the formation of the VXI*plug&play* Systems Alliance with the intent of revolutionizing VXI-based test-system development. The alliance's founders are Red Aylward, Ron Wolfe, Malcolm Levy, David Haworth, and Darrell Johnson. One year after its formation, the alliance has produced nine specifications that standardize common software and system standards and practices far beyond the scope of the original VXI instrument-on-a-card specification. An additional 27 vendors have joined the alliance. Significantly, another group of instrument vendors led by Hewlett-Packard, which was moving in a different direction, joined the alliance last July.

The VXI*plug&play* specifications give test-system developers true "plug and play" interoperability among a wide variety of products, greatly easing the development of multivendor VXI-based systems. Currently, the alliance is developing an I/O driver software standard called the Virtual Instrument Software Architecture (VISA) that will encompass a superset of existing and announced software specifications. VISA will be interface- and platform-independent and will provide backward compatibility with existing drivers.

To vote for this entrant as Innovator of the Year, mark the appropriate box on the ballot.

NATIONAL INSTRUMENTS
AUSTIN, TX
(512) 794-5554

ICs & SEMICONDUCTORS

AD1890 SAMPLEPORT IC

The AD1890 SamplePort IC automatically senses input and output clock frequencies and synchronizes input and output data streams. The device achieves this through asynchronous sample-rate conversion—a technique that uses a universal buffer between sources with incompatible sample rates—and solves the problem of com-

munication between two or more systems acting as clock "masters." At $28.90 (1000), the device replaces multiDSP-based boards that cost between $1000 and $10,000.

The AD1890 uses a sample-rate conversion technique called polyphase filtering. The digital sample sequence goes to a highly oversampled digital FIR lowpass filter with a passband of 0 to 20 kHz. The oversampling takes many thousands of times the number of coefficient samples required to satisfy the Nyquist criterion. Depending on the instantaneous temporal relationship between the input-sample clock events and the output-sample clock events, a sparsely sampled subset of coefficients of this filter processes the input samples. These coefficients, nominally 64, represent a subfilter of the original prototype and have a magnitude response identical to that of the original prototype. The amplitude response has a very flat passband, a steep transition band, and a high degree of stopband attenuation.

To vote for this entrant as IC and Semiconductor Product of the Year, mark the appropriate box on the ballot.

ANALOG DEVICES INC
NORWOOD, MA
(617) 329-4700

TRUEGAUGE MTA11200 BATTERY-MANAGEMENT IC

The TrueGauge MTA11200 battery-management IC provides monitoring and charging control for nickel-cadmium, nickel-metal-hydride, or lead-acid battery packs. The device works by digitally integrating a battery's discharge and charge current to determine the total capacity and state of charge. The IC automatically measures the total capacity and factors it into the state-of-charge calculation. Thus, the device provides an accurate indication of remaining battery capacity.

The MTA11200 performs an automatic total-capacity measurement during battery-conditioning cycles in which the battery cycles from full charge to full discharge. To extend battery life, the IC requests conditioning cycles at regular intervals, determined by battery usage. Additionally, the device constantly monitors battery condition and can transmit battery parameters via a one-wire interface or an optional RS-232 bidirectional serial link. These parameters are remaining capacity, total capacity, voltage, current, temperature, state of charge, and battery error. An 8-bit RISC microcontroller core provides the intelligence in the MTA11200. $3.75 (10,000).

To vote for this entrant as IC and Semiconductor Product of the Year, mark the appropriate box on the ballot.

MICROCHIP TECHNOLOGY INC
CHANDLER, AZ
(602) 786-7200

HC5506D SLIC FOR TELEPHONE-EXCHANGE LINE CARDS

The HC5506 is a subscriber-line interface circuit (SLIC). In either central-office or PBX telephone exchanges, the exchange has a line card connected to every phone line the exchange serves. Thus, exchange sizes are extremely large. Line cards perform telephonic BORSCHT functions, such as detecting when a phone has been picked up, powering the phone, and passing voice signals. The heart of the line card is the SLIC, a linear IC that drives the line, and on which some of the BORSCHT functions have been integrated. As a result of a number of innovations, the HC5506D SLIC allows exchange sizes to be reduced by 30% or more.

The HC5506 integrates the ringer generator relays onto the SLIC. By having a system architecture and power sharing and management techniques that reduce chip power by 50%, the chip allows two SLICs to be placed in one package. In addition, the HC5506 uses novel system blocks to allow line-card components that are so small they are surface mountable. The chip is the only SLIC that removes ringer-generator electromechanical relays. The HC5506, which integrates dual SLICs in a single package, costs $15 (100).

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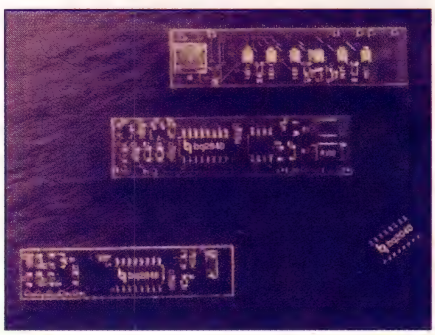
HARRIS SEMICONDUCTOR
MELBOURNE, FL
(407) 724-7862



BQ2040 A/D CMOS IC

Model bq2040 is an A/D mixed-signal CMOS IC that meets the Intel/Duracell System-Management Bus and Smart-Battery Data specifications, providing comprehensive capacity monitoring for lithium-ion, nickel-metal-hydride, and nickel-cadmium batteries. The device provides accurate, repeatable measurement of the available charge in these rechargeable batteries. It performs its function by measuring the charge- and discharge-induced voltage drop across a low-value (10 to 50 mΩ) sense resistor in series with the negative battery terminal. The bq2040 autocalibrates its capacity determination over the life of the battery to provide accurate capacity information over a wide range of operating conditions. The bq2040 is small enough to integrate into a circuit that fits in the crevice between two "A" cells and is housed in a 16-pin, 15-mil SOIC package. A RISC-based CPU, an A/D converter, a V/F converter, a temperature sensor, a timebase, a reference, display drivers, and SM-Bus interface

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Ultra-wideband response achieves low droop and fast risetime for pulse applications. Ratings up to 1000M ohms insulation resistance and up to 1000V dielectric voltage. For wide dynamic range applications involving up to 100mA primary current, use the T-H series. Fully detailed data appear in our 740-pg RF/IF Designer's Handbook.

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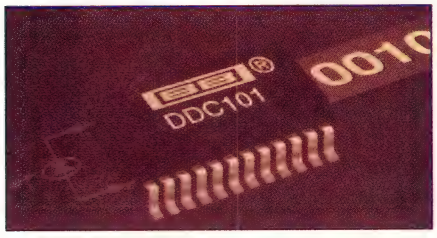
circuitry are integral to the bq2040. The V/F converter can resolve current differences that produce less than 20 μV in the input signal. An internal temperature sensor provides 0.1°K resolution from 230 to >330°K.

You can use an external EEPROM to program initial values into the bq2040. The device accommodates 25 pieces of information in the initial configuration memory, including electrical parameters, the manufacturer's name, serial number, date of manufacture, brand name, and battery chemistry. The bq2040 can drive low-power LEDs directly to display capacity information, which shows the charge state in either absolute or relative mode. In relative mode, the LEDs show the battery charge in 20% increments as a percentage of the full-charge capacity or learned-battery capacity. Depending on the battery's discharge history, the full-charge capacity may be lower than the initial design capacity. In absolute mode, the LEDs display percentage of design capacity in 20% increments with a sixth LED showing an "overfull" condition. The device costs $3.82 (50,000).

To vote for this entrant as IC and Semiconductor Product of the Year, mark the appropriate box on the ballot.

BENCHMARQ MICROELECTRONICS
CARROLLTON, TX
(214) 407-0011



DDC101 A/D CONVERTER

The model DDC101 A/D converter specifically targets direct connection to low-level sensors, such as photodiodes and other current-output devices. The converter replaces an amplifier circuit, a programmable-gain amplifier, and a high-resolution (20-bit) A/D converter. The IC uses a delta-modulation topology with digital integration, oversampling, correlated double sampling, and digital filtering. During conversion, the DDC101 collects the input signal on an internal integration capacitor for a user-determined integration period. A high-precision, autozeroed comparator samples the analog input node. Tracking logic updates the internal, high-resolution D/A converter at a 2-MHz rate to maintain the analog input at virtual ground. A user-programmable digital filter oversamples the tracking logic's output and passes a low-noise, high-resolution digital output to the serial I/O register.

Correlated double sampling (CDS) eliminates steady-state and conversion-cycle-dependent offset and switching errors that conventional analog circuits can't. After the digital filter oversamples the tracking logic's output at the start and end of each integration period, the DDC101 measures the charge accumulated in the integration and performs CDS by subtracting these two data points. The technique eliminates errors, such as charge injection, offset voltage, and reset noise. The integration time depends on the magnitude of the input current. In unipolar mode, the maximum charge the DDC101 can capture is 500 pC. In addition to the normal mode of one integration per conversion, you can configure the device to perform anything from one to 256 integrations per conversion. With multiple integrations per conversion, the DDC101 internally averages the cycles to provide one conversion result. The result, thanks to the averaging, is lower noise. $22.95 (1000).

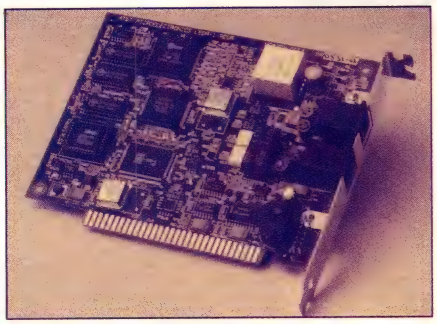
To vote for this entrant as IC and Semiconductor Product of the Year, mark the appropriate box on the ballot.

BURR-BROWN CORP
TUCSON, AZ
(602) 746-1111

V.FLEX HIGH-SPEED MODEM CHIP SET

The software upgradeability of the V.flex chip set will play a significant role in the roll out of V.34 modems. As with any new standard specification, V.34 is subject to varying interpretations by different modem vendors. As a result, many modems will not be interoperable. Modem users and vendors can make the necessary adjustments through software upgrades using V.flex technology.

The complete modem chip set is based on the DSP163x data pump and C882 modem controller. The modem controller subsystem consists of the C882 and external RAM and ROM. The C882 firmware performs the processing of general modem control, AT command set, error correction, data compression, host interface, low power management, and external memory interface functions. A 4k×1-bit serial EEPROM must be used for nonvolatile storage. At the heart of the DSP163x data-pump subsystem is the company's patented ILAD (integrated linear codec and DSP) technology. These mixed-signal DSPs integrate an analog codec onto the same silicon as a DSP1600 core. The HSM288LCF modem chip set is $79(10,000).



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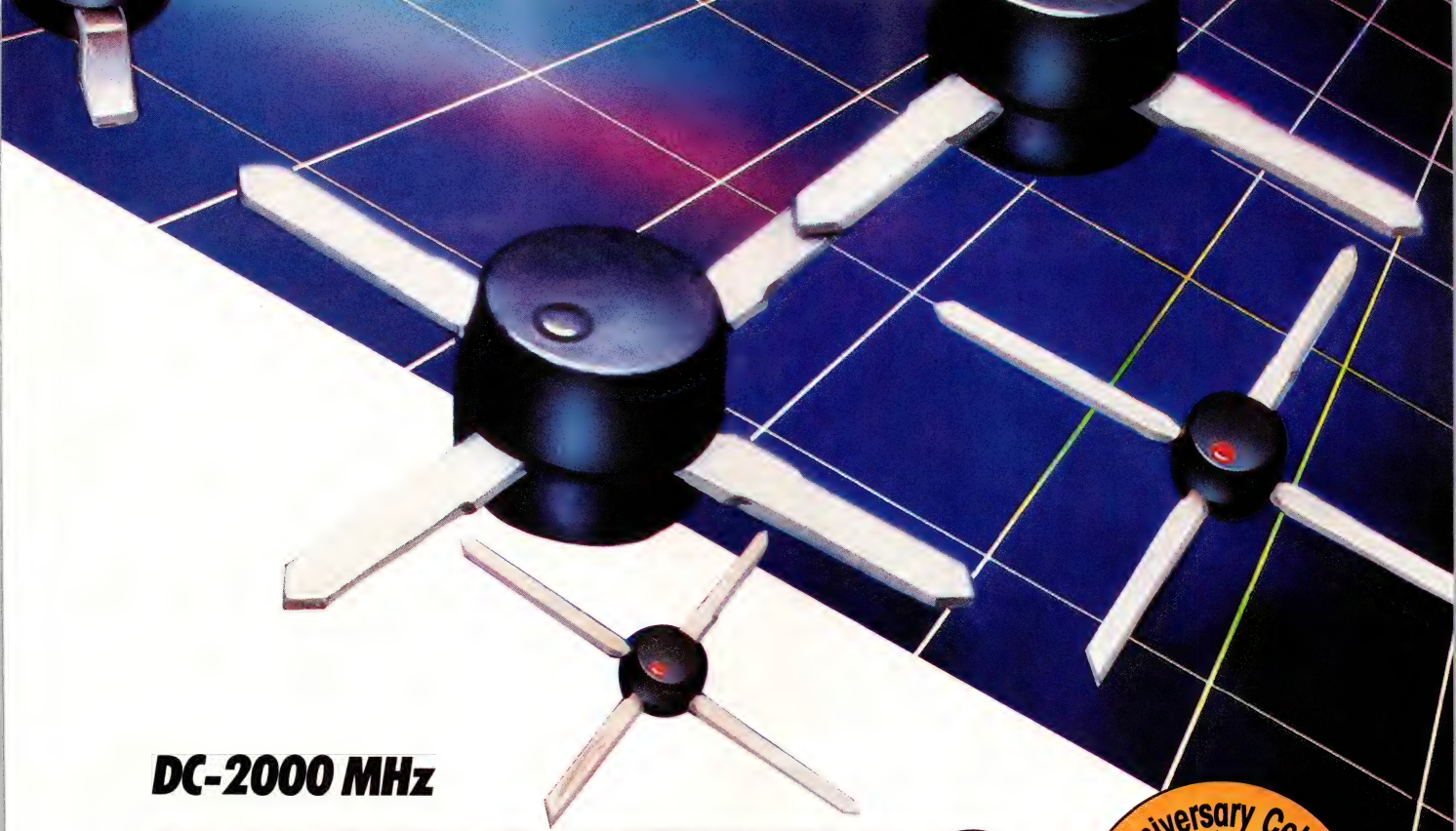
AT&T MICROELECTRONICS
ALLENTOWN, PA
(800) 372-2447

NI1000 RECOGNITION ACCELERATOR

The Ni1000 learns to recognize patterns in data, such as characters, manufacturing defects, financial fraud, or fingerprints. It recognizes these patterns at 32,000 patterns/sec. It achieves this speed with an on-chip parallel, pipelined radial basis function (RBF) neural network made up of five independent functional units: a RBF neural network classifier, a 16-bit RISC μC, a six-stage pipelined math processor, a double buffered input data unit, and an output data formatter/buffer. The classifier contains 512 parallel distance calculating units (DCUs) and a prototype array memory, which stores 1024 vectors in on-chip flash memory using Intel's 0.8-μm CHMOS IV process. The math unit calculates probability densities and results classes simultaneously.

The DCUs simultaneously calculate the city-block distance between a 5-bit feature of an input vector and the corresponding feature of one of two local prototype vectors. A separate on-chip, general-purpose μC supervises the training of the neural network and performs on-chip maintenance and moni-



DC-2000 MHz

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It's just as easy to create an amplifier that meets other specific needs, whether it be low noise, high gain, or medium power. Select from our wide assortment of models (see chart), sketch a simple interconnect layout, and the design is done. Each model is characterized with S parameter data included in our 740 page RF/IF Designer's Handbook or available from our applications department.

All Mini-Circuits amplifiers feature tight unit-to-unit repeatability, high reliability, a one year guarantee, tape and reel packaging for SMD, off-the-shelf availability, with prices starting at only 99¢.

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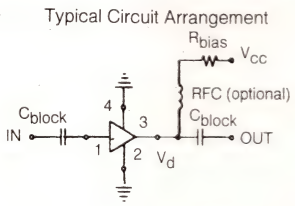
Size (mils)	Value
80x50	10, 22, 47, 68, 100, 220, 470, 680, 1000, 2200, 4700, 6800, 10,000 pf
120x60	.022, .047, .068, .1 µf

Typical Circuit Arrangement



	MODEL	Freq. (MHz) DC TO	GAIN (Typ. dB) At 100MHz	MAX. Power (@ 1dB Compr.) dBm	NF dB (Typ.)	Price $ea. (Qty. 50)
MAR	MAR-1	1000	18.5	1.5	5.5	.99
	MAR-2	2000	12.5	4.5	6.5	1.35
	MAR-3	2000	12.5	10.0	6.0	1.45
	MAR-4	1000	8.3	12.5	6.5	1.55
MAR SM	MAR-6	2000	20.0	2.0	3.0	1.29
	MAR-7	2000	13.5	5.5	5.0	1.75
	MAR-8	1000	32.5	12.5	3.3	1.70
RAM	RAM-1	1000	19.0	1.5	5.5	*6.40
	RAM-2	2000	12.5	4.5	6.5	*6.40
	RAM-3	2000	12.5	10.0	6.0	*6.40
	RAM-4	1000	8.5	12.5	6.5	*6.40
	RAM-6	2000	20.0	2.0	2.8	*6.40
	RAM-7	2000	13.5	5.5	4.5	*6.40
	RAM-8	1000	32.5	12.5	3.0	*6.40
MAV	MAV-1	1000	18.5	1.5	5.5	1.10
	MAV-2	1500	12.5	4.5	6.5	1.40
	MAV-3	1500	12.5	10.0	6.0	1.50
	MAV-4	1000	8.3	11.5	7.0	1.60
MAV SM	MAV-5SM	50-1500	8.0	18.0	6.5	2.07
	MAV-11	10-1000	12.7	17.5	3.6	2.10
VAM	VAM-3	2000	11.5	9.0	6.0	1.45
	VAM-6	2000	19.5	2.0	3.0	1.29
	VAM-7	2000	13.0	5.5	5.0	1.75

*Qty. 10

MAR & MAV MODELS: Plastic flat pack...for surface mount, add SM suffix to model number and 5¢ to price. Example: MAR-2SM...$1.40. MAV-5SM available plastic surface mount only.
RAM MODELS: Ceramic surface mount.
VAM MODELS: Plastic surface mount.

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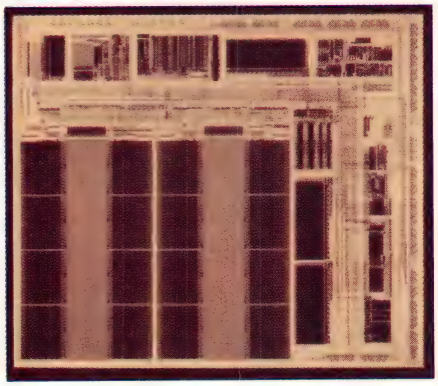


toring tasks. Separate dual-input data buffers and a single output buffer are provided, permitting simultaneous pipelined operation on as many as three input patterns. The output buffer provides several output data formats to support various application requirements, including integer and single-precision IEEE floating-point calculations. $487 (1000).

To vote for this entrant as IC and Semiconductor Product of the Year, mark the appropriate box on the ballot.

NESTOR INC
PROVIDENCE, RI
(401) 331-9640

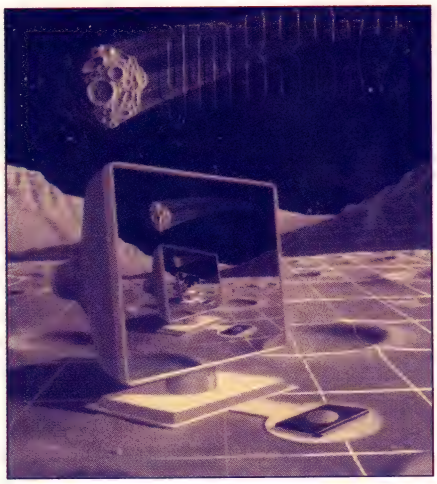
ONEMASK GATE ARRAY

The OneMask family of gate arrays uses a single etch wafer-fabrication process. The technology enables gate arrays with as many as 45K gates and cost-effective production volumes as low as 10 units per shipment. Using the same base wafer and layout as its popular Laser Programmable Gate Array (LPGA) family, the company provides a quick and seamless transition from laser prototyping to initial production. The company's mini-fab has the capability to economically and rapidly process single wafers. The mini-fab can achieve rapid delivery of 10 days for moderate production quantities of as many as 5000 pieces or can sustain scheduled deliveries of hundreds of units per month.

OneMask technology enables you to achieve the full performance and densities found in conventional masked gate arrays without paying the high NRE costs. Devices are available in both 1.2-μm CMOS technologies with densities of 45,000 gates. The 1.2-μm QYH400 series features densities of 2000 to 18,000 gates at toggle frequencies of 200 MHz and as many as 248 I/Os. The QYH 520 series (20,000 gates) in an 84-PLCC package is $171 (100).

To vote for this entrant as IC and Semiconductor Product of the Year, mark the appropriate box on the ballot.

CHIP EXPRESS
SANTA CLARA, CA
(408) 988-2445



ACUITY RESIZING TECHNOLOGY

Acuity Resizing is a core technology that is capable of the real-time resizing of motion and still images. The technology is currently available in 65- and 33-tap architectures. The following ICs realize acuity technology: gm865×1, gm833×2, and gm833×3. The high-end, single-channel gm865×1 chip uses as many as 65-tap filtering independently in both vertical and horizontal directions. For less costly solutions, the gm833×2 offers 33-tap filtering vertically and 33 taps horizontally. The gm833×3 is a triple-channel version of the same part.

Currently, the market's most commonly used resizing technology is bilinear interpolation, which performs poor filtering and introduces unsightly aliasing artifacts. Acuity Resizing chips are more complex and use multirate DSP methodology. Bilinear methods apply only 2 taps of filtering in each direction. Applications for the gm865×1 chip include high-end broadcast equipment, medical imaging, and projection systems. The device makes it possible to zoom into ultrasound images and reveal fine detail on screen. The prices range from $175 (1000) for the gm865×1; to $37 (25,000) for the gm833×2; and $49 (25,000) for the gm833×3.

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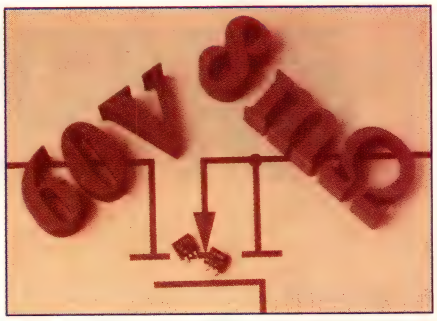
GENESIS MICROCHIP INC
MARKAM, ON, CANADA
(905) 470-2742



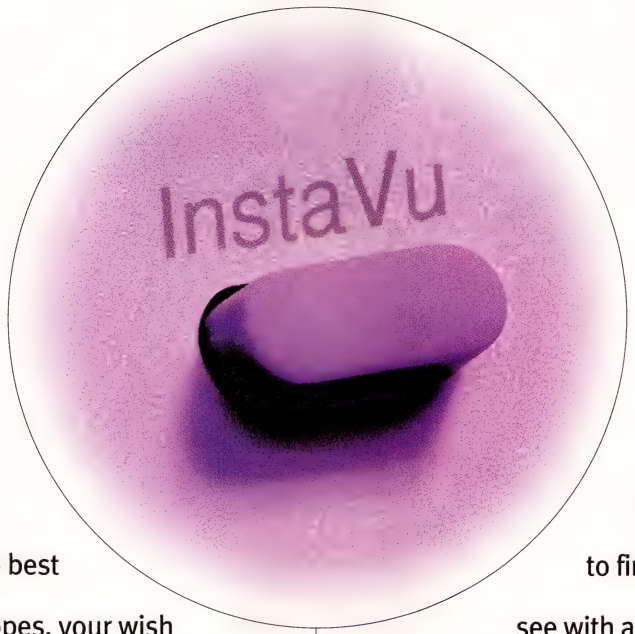
TRENCHFET POWER MOSFETS

The SUB75N06-08 Series of power MOSFETs, called TrenchFET, are 60V devices with 8-mΩ maximum on-resistance and 75A maximum current-handling capability. The SUB75N06-08 comes from the first commercially available vertical-trench power-MOSFET process. The device features cell densities greater than 8 million cells per square inch. The FETs operate at 175°C maximum junction temperature and come housed in TO-220 or -263 packages. The unprecedented low on-resistance drastically reduces heat-sinking requirements in many applications, thereby lowering part count and assembly cost. The low on-resistance and assembly cost also eliminate the need to connect power MOSFETs in parallel.

Although voltage scaling has produced remarkable performance advances in planar DMOS devices, the maximum beneficial cell density faces a barrier. Beyond a certain density, a

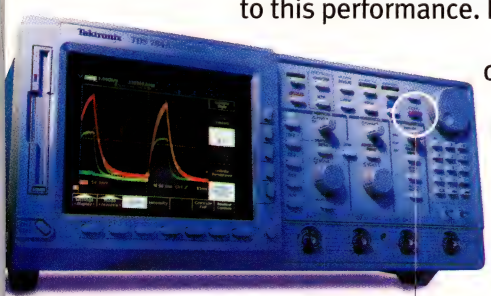
(Continued on pg 45)

Faster than an analog scope. And with instant replay.



If you've ever dreamed of an instrument that combines the best of both analog and digital scopes, your wish has been granted. Tektronix TDS 700A TruCapture™ oscilloscopes are actually faster than the fastest analog scopes. Yet they give you the playback power of digital technology. All at the touch of a button.

Our new InstaVu™ acquisition system is the key to this performance. In a second, it captures glitches that might take other digitizing scopes hours to find. Such as events you could see with an analog scope but were unable to store and review later.



The TDS 700A series gives you true representation of signals, with up to 1 GHz bandwidth and a 4 GS/s sample rate. Plus, it's got the same familiar interface as the entire TDS line so you won't have to learn anything new.

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Tektronix

55A-500053

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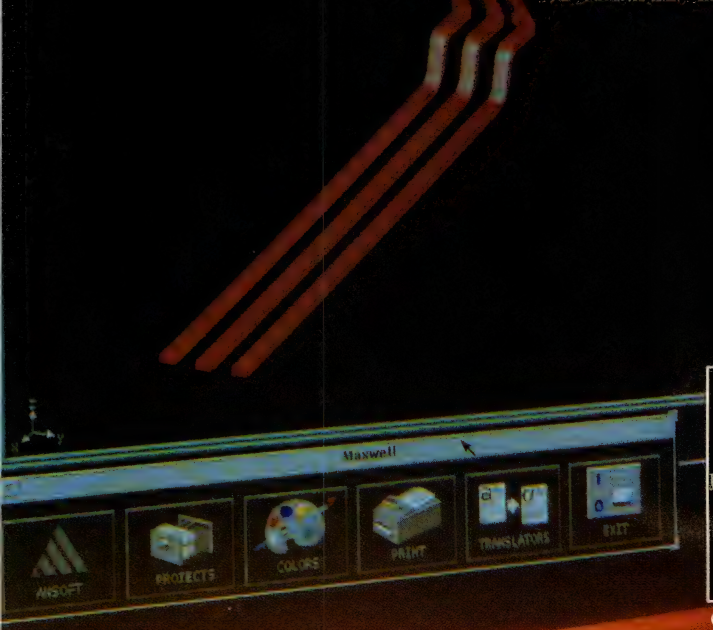
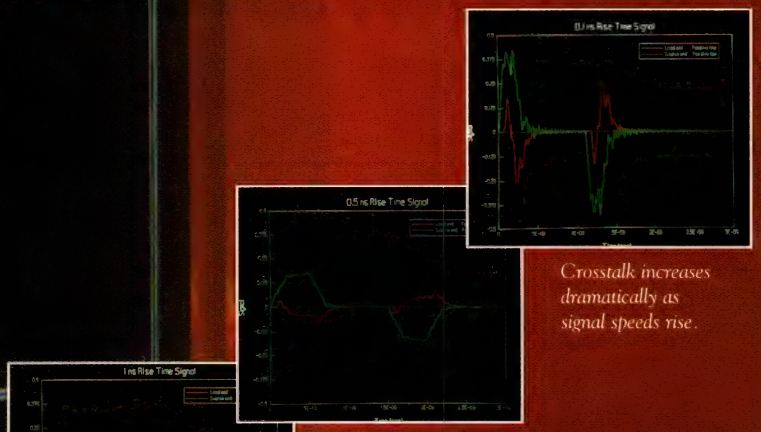
SIGNAL INTEGRITY HEADACHES?





Crosstalk increases dramatically as signal speeds rise.

Courtesy of Motorola, Austin

Crosstalk – Ground bounce – Parasitics – HEADACHES!
As designs get faster, the headache only gets worse.

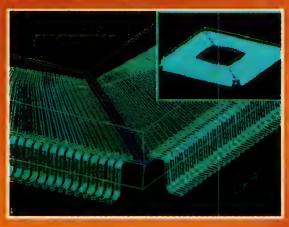
Ansoft has the cure.

1 Proven 3D Extraction

Your designs include packaging, power and ground planes, and multi-layer components – all complicated 3D structures. And nobody does 3D like Ansoft. The 3D field solvers in Maxwell® Spicelink are built on decades of engineering experience and guaranteed correct, accurate answers.

2 Inductance & Non-Ideal Grounds

At clock speeds above 50MHz, inductive effects – such as "ground bounce" – can cripple board, MCM, and package designs. Maxwell offers a proven method of characterizing non-ideal grounds and loop inductance – not partial inductance – so that you KNOW what is happening in your design.



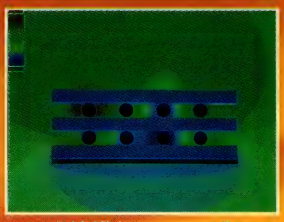
Courtesy of NCR Microelectronics

3 Choice of Extraction Methods

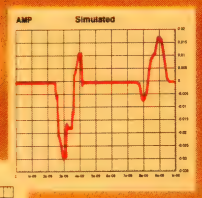
Maxwell gives you all the extraction you need in a single program. Use our fast finite element technology for resistance and inductance calculations, multipole accelerated boundary elements for capacitance calculations, or 2D transmission line or planar simulators for simpler structures.

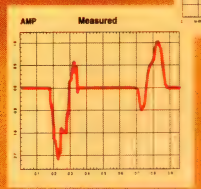
4 SPICE-Level Accuracy

Maxwell Spicelink combines SPICE-level accuracy with accelerated run times on interconnect models. Built-in accelerator for commercial SPICE allows interconnect to be modeled in existing SPICE environments.



Courtesy of AMP Interconnect Systems





5 Experience

Developing genuine cures for signal integrity problems is not easy – others have tried. Join the hundreds of engineers already using our tools to cure their design headaches.

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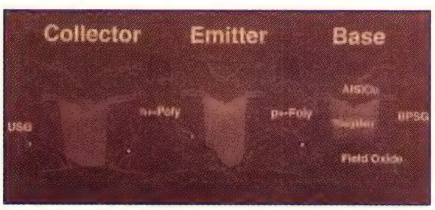
Internet: info@ansoft.com

ICs & SEMICONDUCTORS *(Continued)*

parasitic junction FET, which is intrinsic in the construction of a vertical DMOS device, produces a per-cell increase in resistance that's proportional to cell density. This situation places an upper bound on cell density and limits the lowest value of on-resistance that a planar DMOS FET can exhibit. To overcome this barrier, the TrenchFET structure vertically redirects the current flow in the device's channel in a direct path between the topside source and the backside drain contact. In doing so, the TrenchFET avoids the parasitic series-JFET problem inherent in planar DMOS devices. Process refinements promise to yield devices of steadily increasing density and lower on-resistance, providing the technology suffers no inherent barriers. Curves from the manufacturer extrapolate worst- and best-case densities of 20 and 30 million cells per square inch by the year 2000. Initial devices start at $1.93 (100,000).

To vote for this entrant as IC and Semiconductor Product of the Year, mark the appropriate box on the ballot.

SILICONIX INC
SANTA CLARA, CA
(408) 970-5697



B6HF SILICON-BIPOLAR PROCESS

A novel manufacturing concept allows the B6HF silicon-bipolar process to achieve a cutoff frequency of 25 GHz at V_{CE}=1V, a 1.2-dB noise figure at 2 GHz, a speed-power product lower than 15 fJ, and a minimum current-drive capability of 0.8 mA/μm². The concept involves the use of a CMOS production fab line and several standard CMOS processes and modules. These processes include the company's LOCOS isolation process, a three-level metallization technique, submicron lithography, rapid thermal annealing, layer deposition, and etching. The high-volume CMOS product flow of the wafer fab ensures a high degree of process maturity and low defect density.

Other processes include rapid thermal annealing and a spacer technique, which allows for spacer formation by wet etching without surface erosion of the base areas. The result is an ultrashallow emitter-base doping profile with a base width of only 80 nm. An 0.8-μm lithography with a double-polysilicon self-aligned emitter-base structure produces an effective emitter width of only 0.4 μm, resulting in a low base resistance (low noise) and a low collector-base capacitance (low speed-power product). The high cutoff frequency combined with low collector-emitter voltages make devices produced in the B6HF process especially suitable for 3V, battery-powered handheld systems.

To vote for this entrant as IC and Semiconductor Product of the Year, mark the appropriate box on the ballot.

SIEMENS AG, SEMICONDUCTOR GROUP MUNICH, GERMANY
(011) (49) 89 636-41348

MICROPROCESSORS

NLX220 FUZZY-LOGIC μC

The NLX220 is an inexpensive, self-contained fuzzy-logic μC with analog inputs and outputs that allow you to design the device directly into analog control loops with no additional components. In operation, the μC reads voltage levels from its four analog inputs using an 8-bit A/D converter, processes the channel data using fuzzy-logic rules contained on chip, and generates four analog outputs via its 8-bit D/A converter and four sample-and-hold output drivers. Fuzzy-logic processing at a decision rate of 500,000 rules/sec allows the NLX220 to perform first-, second-, and third-order derivative control; automatic calibration; and rule-based timing at 10,000 samples/sec for each of the four analog channels. The processor uses the "max or min" function to select the appropriate rules from as many as 50 rules stored in its on-chip 256-byte EEPROM. The one-time-programmable version costs less than $2 (1,000,000).

Because you program the NLX220 using fuzzy-logic rules instead of an algorithmic programming language, you can better focus on solving your application problem and spend less time writing lines of code. Rule-based programming eliminates the traditional cycle of compiling, linking, and debugging. You simply focus on the rules of the application at hand. The NLX220 supports six different constant-slope membership functions and can implement floating membership functions, which, based on the incoming data, allow the center and width of any membership function to float dynamically. Customers already using the device claim to have finished designs in a quarter of the time required to program more traditional processor-based control systems. Example applications for the NLX220 include intelligent battery charging, automatic gain control, pattern recognition, closed-loop process control, and temperature control.

To vote for this entrant as Microprocessor Innovation of the Year, mark the appropriate box on the ballot.

AMERICAN NEURALOGIX INC
SAN JOSE, CA
(408) 383-7200

HYPERSPARC MDP

Using advanced silicon-substrate multichip-module technologies and optimized microarchitectural partitioning, the hyperSPARC MDP (multidie package) packs a 110-MHz, 6M-transistor CMOS processor with 256 kbytes of second-level cache memory into one 131-pin PGA package. The chip set consists of the processor, a cache controller and memory-management unit, and four custom SRAMs. Intelligent partitioning of the various CPU functions has removed the interchip delays from critical speed paths so that the six chips operate as a 6M-transistor monolithic device while staying within current IC-manufacturing capabilities. Because the chips comprising hyperSPARC are linked using a silicon substrate, the resistive and capacitive parasitic loads are a fraction of what they would be if the devices were individually packaged and mounted on a pc board. Further, the reduced loading allows for less "guard-banding" of the individual dies, which boosts individual die yield and drops the power consumption of the completed product.

The hyperSPARC MDP is an enhancement of an existing design. Earlier versions of hyperSPARC were fabricated in a 0.65-μm, two-level-metal process. Migration to a 0.5-μm, three-level-metal fabrication process

reduces the die size by 40%. Coupled with the change from individual TAB (tape-automated-bonding) packages mounted on a pc board to the silicon-substrate MCM, the processor's maximum clock rate has jumped from 72 to 110 MHz. For even more processing speed, you can connect multiple hyperSPARC MDPs without glue logic.

To vote for this entrant as Microprocessor Innovation of the Year, mark the appropriate box on the ballot.

ROSS TECHNOLOGY INC
AUSTIN, TX
(512) 892-7802

PIC16C74 8-BIT μC

The PIC16C74 is a highly integrated, 20-MHz, 8-bit μC that offers designers a one-time-programmable (OTP) device for approximately 30% more than the ROM-based version. Other OTP μCs typically cost twice as much as their ROM-based equivalents—or more. The PIC16C74 includes 4k 14-bit words of EPROM-based program space, 192 bytes of data RAM, an 8-channel, 8-bit A/D converter, a 5-Mbps USART (universal synchronous/asynchronous receiver/transmitter), a timer subsystem with three programmable timers and two input channels, a synchronous serial port that supports the I^2C and SPI serial protocols, a watchdog timer, and built-in power-on reset circuitry. A 4-MHz OTP version of the device costs $5.95 (1000).

Combining a reduced instruction set and Harvard architecture allows the PIC16C74 to deliver 5 MIPS at 20 MHz. The μC can fetch and execute one 14-bit instruction word during each instruction cycle. All instructions execute in one machine cycle except for branches, which require two cycles. Further, the entire 192-byte data RAM serves as the μC's register set, allowing significant compaction of program code and eliminating the need for most data-movement operations. The PIC16C74's A/D converter employs a patented low-power technology using a capacitive-ladder and successive approximation. This low-power technology allows the μC, including the A/D converter, to operate on 3V. The converter can operate from its own RC oscillator so that you can stop the μC's other clocks and put the processor in a sleep state. The converter can then perform the conversion, generate an interrupt, and wake the CPU. Sleep mode can save quite a bit of system power and has the added benefit of increasing conversion accuracy by reducing overall switching noise on the chip.

To vote for this entrant as Microprocessor Innovation of the Year, mark the appropriate box on the ballot.

MICROCHIP TECHNOLOGY INC
CHANDLER, AZ
(602) 786-7200

68060 μP

The 68060's superpipelined, superscalar RISC-hybrid architecture brings the 68000's venerable instruction set into the performance domain of modern 32-bit processors. Its advanced architectural features include a branch cache architecture, a dual-pipeline structure decoupled from the instruction stream by a FIFO stage, a superscalar implementation, and a write-back cache buffer. The μP employs hardwired logic to implement the 68040 instruction set instead of microcode. An instruction buffer separates a four-stage instruction-fetch unit from the two four-stage integer-execution pipelines and the extended-precision floating-point unit (FPU). The instruction-fetch unit contains a 256-entry branch cache memory and uses a five-state prediction model to predict program flow. The instruction-fetch unit converts the incoming stream of variable-length 680x0 instructions into a fixed-length, RISC-executable form. The instruction-fetch unit also removes correctly predicted branches from the instruction stream using a technique called branch folding. The instruction buffer dispatches the instructions from the fetch unit to the appropriate execution units. The 68060's architecture can retire as many as four native 680x0 instructions per clock cycle: two integer instructions, one branch instruction (absorbed by the instruction-fetch unit), and one floating-point instruction. This parallelism provides high execution speeds even for code not specifically recompiled for the 68060's architecture.

There are already three members in the 68060 family. The M68060 includes both a paged memory-management unit (MMU) and a floating-point unit. The M68LC060 includes the paged MMU but not the FPU. The M68EC060 includes neither the MMU nor the FPU. The three processors cost $263, $169, and $150 (10,000) for 50-MHz versions.

To vote for this entrant as Microprocessor Innovation of the Year, mark the appropriate box on the ballot.

MOTOROLA INC
MICROPROCESSOR PRODUCTS GROUP
AUSTIN, TX
(512) 891-2917

cMCU370 MIXED-SIGNAL MICROCONTROLLER FAMILY

The cMCU370 family mixed-signal μCs combine traditional analog circuitry with a CPU core, μC peripherals, and power drivers on a single chip. The family results from a joint development project between Texas Instruments and Delco Electronics. Designers developed the cMCU family using a modular approach, which enables application-specific configurations. The modular library includes two CPU cores (8 and 16 bit); various RAM, EEPROM, and ROM modules; a variety of linear and power modules; and multiple customer-specific modules. Incorporating this technology, the Dashboard Demo Unit, which is the first single-chip dashboard controller for the automotive industry, is currently sampling.

The μC family consists of both software and hardware development tools. An ANSI C compiler translates ANSI C language code into assembly-language code. Once the algorithm is coded in C, the compiler generates the code to be assembled and linked by TI's assembler/linker. Software tools include the C8 or C16 Assembler/Linker PC, $550; C8 or C16 assembler and linker Unix, $1200; C8 or C16 compiler PC, $1950; and C8 or C16 compiler Unix, $2950. Hardware tools include C8 or C16 compact development tool, $2100; and C8 or C16 extended development system, $4000.

To vote for this entrant as Microprocessor Product of the Year, mark the appropriate box on the ballot.

TEXAS INSTRUMENTS
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(317) 451-0940

(Continued on pg 50)

THE WORLD'S MOST ACCURATE HIGH SPEED 10-BIT A/D.

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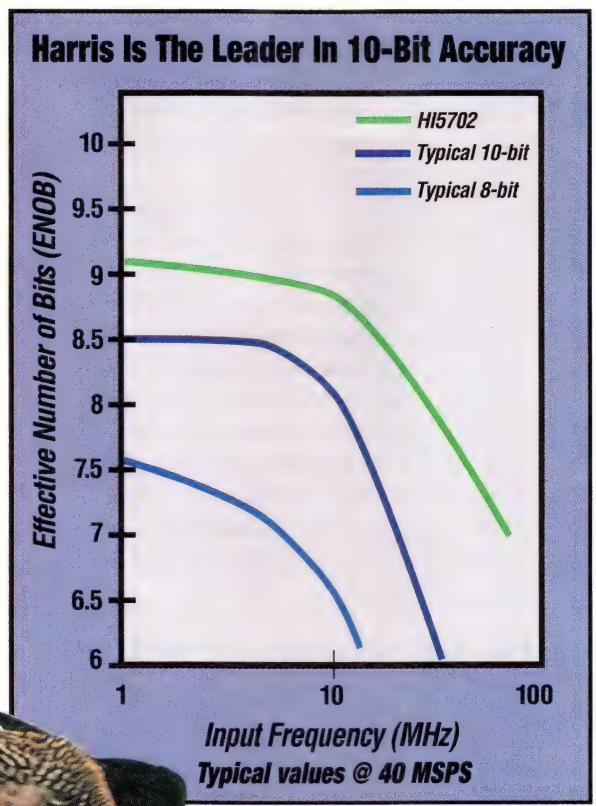

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HARRIS SEMICONDUCTOR

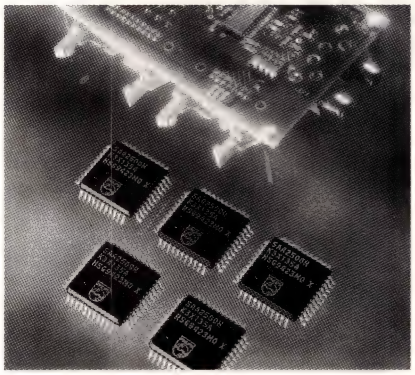
CIRCLE NO. 4

Philips Semiconductors **Update**

Low power MPEG decoder suits a wide range of digital audio applications

The SAA2500 has been introduced to meet market demand for a high-performance MPEG decoder for use in equipment such as digital radios, video disc and CD-i players and multimedia PCs. Incorporating master and slave MPEG data inputs, automatic sample frequency and bit-rate detection, full MPEG-1 layer 1 and 2 decoding, advanced error protection and audio post-processing, the SAA2500 offers the highest level of functional integration currently available in an MPEG decoder. Packaged in a 10 mm square 44-pin quad flat pack and drawing only 26 mA from a 5 V supply, it is ideal for use in battery-powered portable equipment.

The device's master and slave inputs, plus its automatic sample frequency and bit-rate detection, permit its use in a wide variety of applications where MPEG sources with different clock rates need to be decoded. Errors in the incoming bitstream are automatically detected either by examining the syntax of each data frame or by CRC checking. Error flag inputs on the SAA2500's master and slave interfaces can be driven by external processors to indicate data errors, while a separate 'unreliable data' input can be used to interrupt decoding and mute the output.



The new SAA2500 MPEG audio source decoder provides a unique combination of high performance, small size and low power consumption.

The on-chip post-processor applies the digital de-emphasis specified in the MPEG signal and provides a fully-programmable volume control with 0.5 dB smoothed step resolution plus a programmable channel mixer. The SAA2500 supports all the audio modes, bit rates and sample frequencies of MPEG-1 layers 1 and 2 and has a selectable output precision of 16, 18, 20 or 22 bits.

Call 1-800-447-1500 Ext 1173
Europe: circle no. 40

For more information on any of these subjects: call 1-800-447-1500 and request appropriate extension number.

Europe – use EDN Information Retrieval Service or contact us direct via fax on +31 40-724825.

All Philips Semiconductors plants worldwide are ISO 9000 certified

Square-pixel digital video to NTSC/PAL encoder

The SAA7187 is a square-pixel digital video encoder that simultaneously encodes MPEG decompressed data or digital YUV video data into NTSC or PAL composite video baseband and S-video signals with an on-screen display and closed captioning. Designed as an integral part of Philips' DTV chipset, it allows digitally-processed video and graphics information to be displayed or recorded on standard TV or VCR equipment. The device is targeted at PC, workstation, motherboard and add-on board manufacturers incorporating video playback into their product; it also has applications in live video editing and processing systems.

The new IC provides three 8-bit-wide data ports accepting the pixel data in various formats: the VP1 port accepts eight lines of multiplexed Cb-Y-Cr data (CCIR-656 mode), or Y-data only (444 or 422 mode); the VP2 port accepts Cr-data in 444 input mode; and the VP3 port accepts Cb-data (444 input mode) or multiplexed Cb/Cr data (422 mode). When not used for video input data, this port can also handle the data of an 8-bit-wide microprocessor interface. The SAA7187 also includes a 3-pin input port with look-up tables for an on-screen display.

The SAA7187 accepts differently formatted YUV data with 640 or 768 pixels per line. Pixel frequency can be either 12.27 MHz (60 Hz fields) or 14.75 MHz (50 Hz fields). It has I²C-bus and MPU parallel control ports and may be run in master or slave mode.

The SAA7187 contains three 10-bit oversampled DACs producing composite video and s-video outputs simultaneously. It operates off +5 V and is packaged in a 68-pin PLCC package.

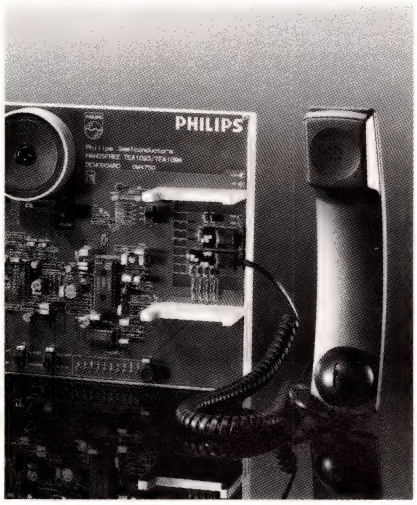
Call 1-800-447-1500 Ext 1175
Europe: circle no. 41

Philips Semiconductors

New high-performance hands-free telephone IC

The latest addition to the Philips range of hands-free telephone ICs, the TEA1094, is optimized for use in mains and battery powered equipment. It features all the hands-free functions required in a telecom terminal, including microphone and loudspeaker amplifiers, duplex controller with speech and background noise envelope monitors, channel switching logic and muting facilities.

The TEA1094's normal operating parameters, including its transmit/receive gain, sensitivity and timing, are easily adjustable using external passive components, and it interfaces directly to



The new TEA1094 hands-free telephone IC is optimized for use in mains or battery powered equipment, while the existing TEA1093 is intended primarily for line-powered systems.

speech/transmission circuits such as Philips' TEA1060 family and PCA1070 ICs. It is suited for use in a wide range of equipment, such as speaker phones, cordless phones, fax machines, answering machines and intercom systems.

The loudspeaker amplifier has a powerful single-ended output stage with a unique rail-to-rail voltage swing that allows it to deliver up to 45 mW of output power (12 V supply, 8 Ω loudspeaker). Amplifier gain can be programmed over a 0 to 33 dB range via a single external resistor, while a low-cost linear potentiometer is all that is needed to provide logarithmic volume control. The microphone amplifier's nominal gain is also programmable via an external resistor over the range 0 to 31 dB.

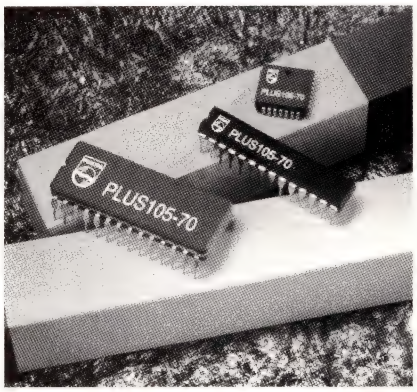
Call 1-800-447-1500 Ext 1172
Europe: circle no. 42

Upgraded programmable state machine supports highly complex state sequences at rates up to 100 MHz

Philips Semiconductors has introduced an upgraded version of their programmable logic sequencer, the PLUS105-70, which can process highly complex state transition sequences at rates of up to 100 MHz. This classic Mealy state machine has a clock rate that can support pipelined state machines, operating at 100 MHz ($f_{internal}$). The operating frequency of the PLUS105 is 70 MHz (f_{max}), assuming data originates at the inputs, is stored, and is then clocked out through the output registers.

The PLUS105-70 is a fully synchronous state machine which has both buried state registers and output registers. It is ideal for complex timing and control functions such as bus interface, interrupt vector generation and decode, memory control and interface protocol control. Applications include video graphics inputs, workstations, mainframes, telecommunications and any high-performance EDP.

Because the feedback path of the buried registers is internal to the PLUS105-70, intermediate state transitions can be stored or fed back without tying up pins for feedback, effectively doubling device capacity compared with more conventional PALs. The two fully-



The PLUS105-70 programmable state machine is available in three different packages: 28-pin PLCC and both 300-mil and 600-mil-wide dual in line.

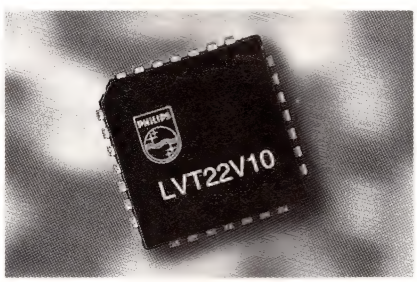
programmable arrays, and J-K registers, provide greater flexibility too. The PLUS105 user programmable OR array supports 100% product term sharing without stealing or borrowing AND terms from other registers. Accordingly, any one or all of the 48 AND terms can be connected to any or all of the 16 registers.

Call 1-800-447-1500 Ext 1171
Europe: circle no. 43

Fastest 3.3 V PLD provides high performance with low output noise

The new LVT22V10-7 3.3 V PLD is a 7.5 ns device that gives designers the speed required to keep up with the increasing performance of leading 3.3 V microprocessors and memory devices.

The LVT22V10-7 provides speed as well as key features that are essential for high-performance systems including low noise, high drive, 3.3



The LVT22V10-7 is the industry's fastest 3.3 V PLD, the latest in a series of high-performance PLDs from Philips.

and 5 V compatible inputs and outputs, live insertion and graceful power-up for the design engineer concerned about quality system implementation.

The device has virtually no ground bounce with only 0.8 V V_{olp} under worst-case conditions (one output held low and nine outputs switching, each with a 50 pF load at 3.6 V). With system clock rates at 90 MHz and above, noise becomes a critical design consideration and the LVT22V10-7 decreases output noise by 50% compared with CMOS PLDs.

The LVT22V10-7 is the fastest in a series of high-performance 3.3 V programmable devices from Philips. It joins the LVT22V10-10 and LVT22V10-15, which are 10 ns and 15 ns devices respectively.

Call 1-800-447-1500 Ext 1174
Europe: circle no. 44

2/95/US

PHILIPS

FLASHDSP 1616 WITH ON-CHIP NONVOLATILE FLASH MEMORY

The FlashDSP 1616 is a DSP chip that sports an on-chip nonvolatile flash memory. The FlashDSP chip has the same feature set as the DSP1616-x30 Piranha DSP chip. The chip operates from 5 and 3V. It contains 12 kbytes of flash memory and delivers as many as 50 MIPS at 5V and 30 MIPS at 3V. Incorporating an on-chip flash memory where ROM is usually found enables you to bring products to market faster. The product combines flash-memory technology with 0.6-μm digital technology.

The chip provides nonintrusive in-system programmability. Currently, engineers typically develop a prototype system with external SRAM for the software use, then they redesign the circuit to use ROM-encoded DSP for production. In parallel, the software engineer submits software for ROM encoding, which typically takes 6 to 12 weeks. With the FlashDSP, an engineer only needs to design the DSP or ROM-encoded processor. Designers develop software on the production board design, thereby reducing the complexity of developing DSP-based products. A chip operating 50 MIPS at 5V costs $1000 (to 10 units).

To vote for this entrant as Microprocessor Product of the Year, mark the appropriate box on the ballot.

AT&T MICROELECTRONICS
ALLENTOWN, PA
(610) 712-7278

68356 EMBEDDED μP

You can classify the 68356 Signal Processing Engine as an embedded μP or as an integrated communications processor. The device's primary function is to provide embedded-system designers with a highly integrated processor. The 68356 accomplishes this task by having three independent processors integrated into the design. The processors include a 68000 core processor, a RISC-based communications processor, and the 32-bit 56002 DSP core. The 68000 offers you use of an industry-standard, general-purpose μP, and the DSP 56002 provides high DSP performance. The RISC-based communications processor provides an intelligent serial-communications peripheral with three multiprotocol serial-communications channels (SCCs).

The RISC processor frees the 68000 from having to manage SCC tasks. In addition, to minimize glue logic, the 68356 includes an interrupt controller, three timers, chip selects, clock generators, a DMA controller, and three communication paths between the 56002 and the 68000. The cores are fully static, allowing for power management. Also included onchip is a large array of DSP RAM (5.5k×24 program, 3k×24 X-data, and 2.5k×24 Y-data). The 68356 chip costs $64.95 (10,000).

To vote for this entrant as Microprocessor Product of the Year, mark the appropriate box on the ballot.

MOTOROLA INC
SEMICONDUCTOR
PRODUCTS SECTOR,
AUSTIN, TX
(512) 891-2429

TMS320C80 DSP CHIP

The TMS320C80 single-chip multiprocessor combines parallel DSP and RISC architectures and performs more than two billion operations per second (BOPS). This single-chip multiprocessing DSP is capable of multitasking several compute-intensive real-time functions. The chip's two-BOPS performance lets you replace multiple-processor or multiple-board solutions in many systems. The TMS320C80 integrates four million transistors; four advanced DSPs, which employ a 64-bit instruction word; a 32-bit RISC master processor with a 100-Mflops FPU; and a high-throughput DMA designed to deliver real-time performance- and data-hungry applications, such as video, imaging, and graphics.

In addition, because the chip is fully programmable, it allows you the flexibility and power to combine industry-standard and proprietary algorithms. For example, the TMS320C80 is the only single chip available that can concurrently support the entire H.320 video-conferencing standard. Other algorithms the chip supports include MPEG and JPEG. The company also enhanced its TMS320 tools by developing optimizing compilers and algebraic assemblers for the chip. Other tools include device and system simulators and a full-screen-emulation unit. The chip costs $400 (10,000).

To vote for this entrant as Microprocessor Product of the Year, mark the appropriate box on the ballot.

TEXAS INSTRUMENTS
STAFFORD, TX
(713) 274-3377

TEST & MEASUREMENT

700A SERIES DSOS

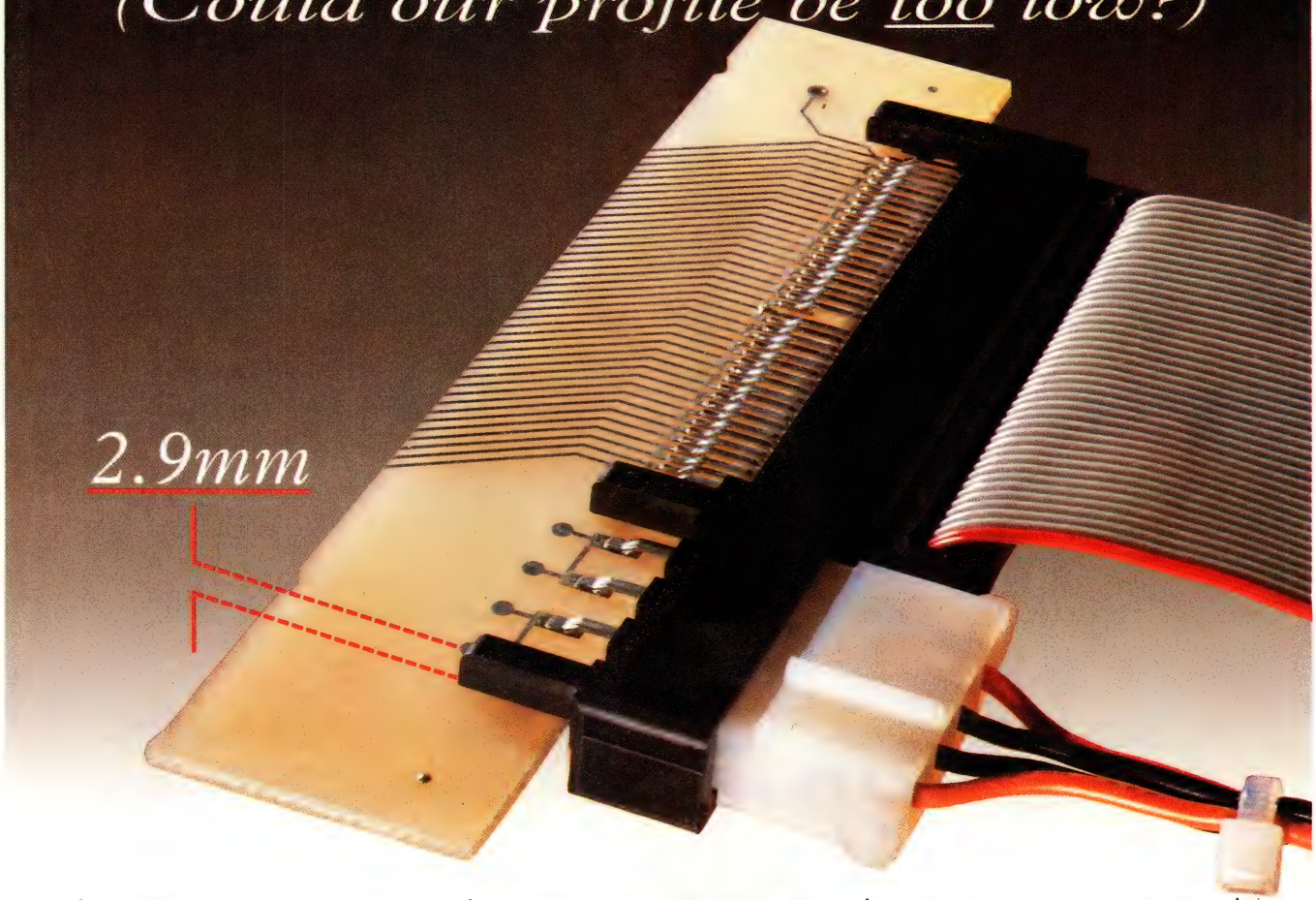
Thanks to a feature called InstaVu, the four-channel digital storage oscilloscopes (DSOs) in Tektronix's TDS 700A series acquire as much data in 1 sec as other high-performance digital scopes acquire in an hour. If you're trying to find elusive anomalies in waveforms that are nearly always normal, the time that InstaVu can save you is dramatic: The feature increases by a factor as great as several thousand the likelihood that an anomaly will occur while the scope is capturing a waveform, rather than in the dead time between sweeps. The 1-GHz-bandwidth TDS 784A ($34,495; $39,690 with four active probes) takes 4G samples/sec in single-channel mode—one of the fastest real-time sampling rates available. But what's so remarkable is not the sampling rate but the scope's ability to acquire over 400,000 waveforms/sec. Normally, even the fastest-sampling DSOs acquire only a few hundred waveforms/sec. (Tek's TDS 544A, the predecessor of the $17,750, 500-MHz-bandwidth TDS 744A, includes a 50,000-waveform/sec mode called FastFrame. The TDS 700A scopes include FastFrame as well as InstaVu.)

Capturing ephemeral waveform aberrations has been the province of specialized analog scopes whose CRTs include electron-multiplying plates. Using those scopes has involved staring into a viewing hood at a bright trace in the hope of sighting faint and fleeting anomalies. With InstaVu, the picture is sharp, clear, and color-graded to indicate how often the anomalies occur. What makes InstaVu possible is a new

(Continued on pg 55)

NOT MANY PEOPLE KNOW THAT IBM USE OUR NEW COMBI-CONNECTOR

(Could our profile be too low?)



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CIRCLE NO. 96

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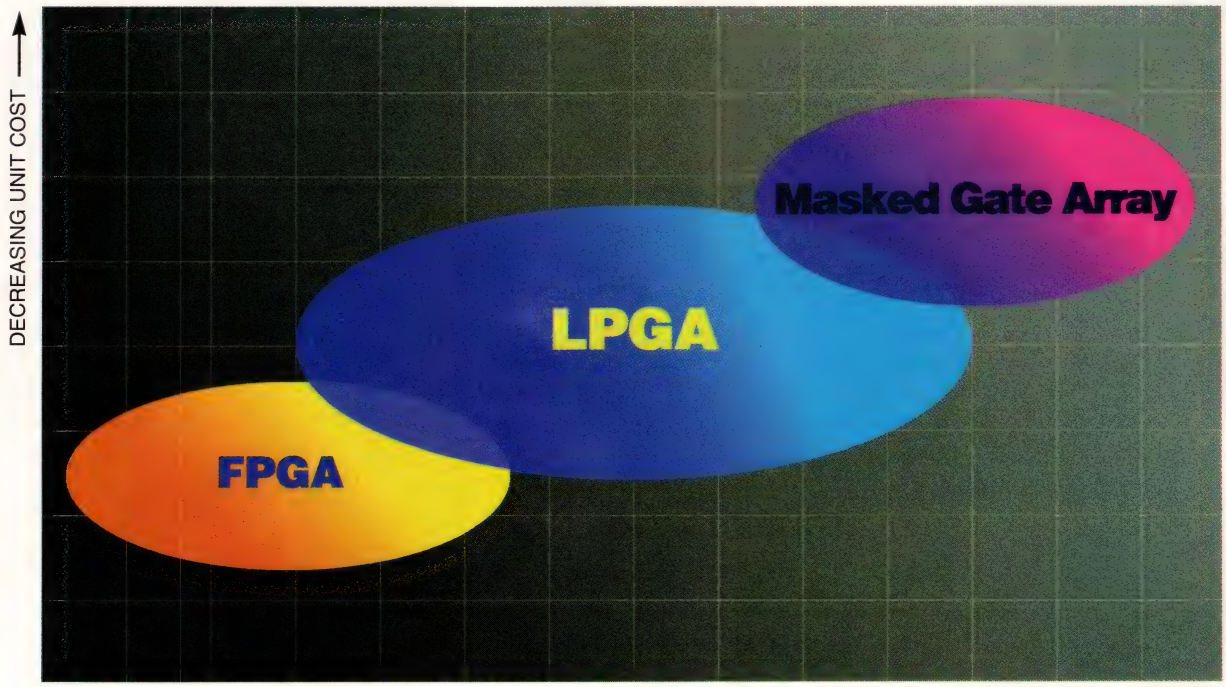

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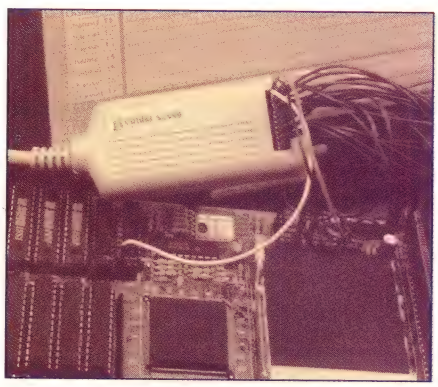
CIRCLE NO. 87

architecture embodied in a CMOS ASIC. This IC contains as many transistors as Intel's Pentium μPs but dissipates only 2.5W while processing 1 Gbyte/sec. The device converts thousands of waveforms into a single bit-mapped screen image before transmitting the information to the display subsystem. As a result, the information-transfer rate is only about 400 kbytes/sec instead of over 200 Mbytes/sec.

To vote for this entry as Test and Measurement Product of the Year, mark the appropriate box on the ballot.

TEKTRONIX INC
BEAVERTON, OR
(800) 426-2200



POD A LYZER 100-MHz LOGIC ANALYZER

The $1295 Pod A Lyzer 8020 performs 80% of the functions of a benchtop logic analyzer, for which you might expect to pay at least $5000. The 0.7×1.5×3.5-in., less-than-1-lb unit plugs into a PC's serial port and comes with Windows-based software. It incorporates a 64-kbit trace buffer for each of its 18 channels. The buffer depth is eight to 16 times that of most PC-based logic analyzers. Most of the other units take up an ISA bus slot; the Pod A Lyzer 8020 doesn't. It plugs into any of a PC's four COM ports, so it works even with notebook PCs. In asynchronous mode, the unit captures 1k to 100M samples/sec on all channels; in synchronous mode, the top speed for qualified captures is 80M samples/sec.

The unit specs a setup time of 2.1 nsec and a hold time of zero. Typical input impedance is 100 kΩ in parallel with 10 pF. The input voltage range is –3 to +7V; thresholds are 1.4V for TTL and 2V for CMOS. Both clock and trigger outputs are available. You must provide the unit with 5V-dc power at 650 mA.

To vote for this entry as Test and Measurement Product of the Year, mark the appropriate box on the ballot.

BOULDER CREEK ENGINEERING
SARATOGA, CA
(408) 867-8170

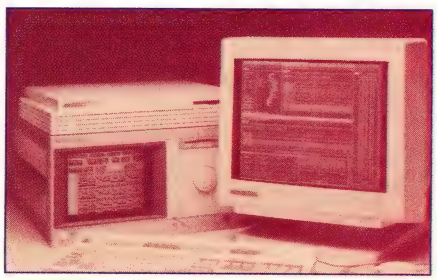
HP54620A LOGIC ANALYZER

One way to characterize HP's 54620A is to call it a $2995, 16-channel logic-timing analyzer for people who have always done digital troubleshooting with a scope. Many people have found that learning to use a logic analyzer is simply too time-consuming. So they continue to use a scope, even though, once they became familiar with the logic analyzer, they could get the job done much faster. HP bases the instrument's design on that of the highly successful 54600 family of low-cost digital storage oscilloscopes. After extensive market research, the designers stripped away some of the more arcane features of high-performance logic analyzers. The result is a unit that—at its fastest sweep speed—takes 500M samples/sec (2-nsec resolution), captures 3.5-nsec glitches at any sweep speed, offers a delaying sweep and split-screen display like those familiar to most scope users, and includes a triggering system that is both flexible and easy to understand. The analyzer triggers on signal edges from any channel or from an external source, on high/low/don't-care patterns from all channels, logical combinations and sequences of patterns, and patterns that repeat for a specified number of times or a specified interval.

The analyzer's cursor- and automatic-measurement modes should be familiar to scope users. Another feature helps you keep track of the meanings of the many displayed signals; a labeling facility lets you select signal names from a menu of standard names augmented by the 85 names you defined most recently. The unit groups its 8-pF-capacitance inputs into a pair of eight-channel pods.

To vote for this entry as Test and Measurement Product of the Year, mark the appropriate box on the ballot.

HEWLETT-PACKARD CO
PERSONAL MEASUREMENTS OPERATION,
LOVELAND, CO
(800) 452-4844



INTEGRATED WORKSTATION/LOGIC ANALYZER

Add significant computing power to a high-end logic analyzer, and you have a tool that can reveal much more about the system you are debugging than the most powerful logic analyzer can on its own. Teaming Hewlett-Packard's new 16505A prototype analyzer ($4995) with the 16500B modular logic-analysis system augments the logic analyzer with a Unix workstation that includes a large-screen color display and dedicated software. With the combined package, you can answer "what-if" questions about your target system's performance *after* you capture the data. Often, this saves setting up an experiment and repeating it again and again. Perhaps most unusual is the system's ability to provide—retrospectively—new views of data you've already acquired. Say you use the timing-analysis mode to capture a trace of an anomalous occurrence. This system lets you reconstruct, after the fact, a time-correlated state-analysis view of that occurrence. If you're dealing with performance anomalies that show up only infrequently, this capability can save lots of time.

The idea of combining computing power with a logic analyzer isn't new. Over the years, several analyzers have done just that. Almost 20 years ago, you could buy a logic analyzer built around a microcomputer that ran the CP/M operating system. But such analyzers

did not use their computers to provide new views of previously captured data.

To vote for this entry as Test and Measurement Product of the Year, mark the appropriate box on the ballot.

HEWLETT-PACKARD CO
COLORADO SPRINGS, CO
(800) 452-4844

PC-415 EISA ADC BOARDS

The customary way to build PC data-acquisition boards that take more than about 1M samples/sec is to design the boards with lots of memory. That way, despite the ISA bus's limited bandwidth, the ADCs can acquire samples in quick succession—until the onboard memory fills. At that point, sampling stops and the stored data travel over the ISA bus to the PC's main memory or to a mass-storage device (the PC's hard disk, for example). The VMEbus is fast enough to break this bus-bandwidth bottleneck, but its price puts it in a different league from standard PCs. The EISA bus also breaks the bottleneck, but it does so at significantly lower cost.

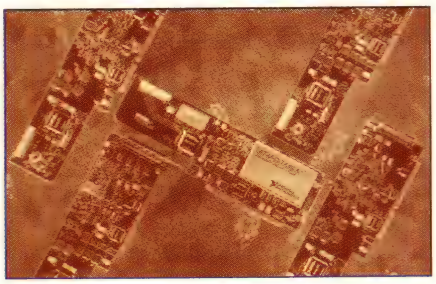
Datel Inc's PC-415 series harnesses the EISA bus's high bandwidth to transmit as many as 14M samples/sec of up to 16 bits. (In other words, transfer rates are as high as 28 Mbytes/sec.) The boards stuff two samples into a 32-bit transfer. Many EISA PCs accommodate 64 Mbytes of RAM, so the PC's main memory can store records of substantial length. Moreover, by tagging events of interest, the boards make such events easier to locate in the long records. Among the series' eight 12- and 14-bit models are two 12-bit units: a $1925, four-channel board whose ADC converts in 500 nsec and a $2495, single-channel, 10M-sample/sec board.

To vote for this entry as Test and Measurement Product of the Year, mark the appropriate box on the ballot.

DATEL INC
MANSFIELD, MA
(508) 339-3000

AT-MIO-16E-2 EQUIVALENT TIME-SAMPLING BOARDS

ISA bus data-acquisition boards that acquire signals whose bandwidth ranges into megahertz regions have been available for several years. A few boards even use equivalent-time sampling (ETS) to accurately digitize repetitive signals containing high-frequency components that would cause aliasing if sampled at the ADC's normal maximum rate. However, most such boards cost over $2000 or lack features expected in "mainstream" products. Now, though, National Instruments' AT-MIO-16E-2, a full-featured unit priced at $1595, uses ETS to acquire 3-MHz signals—even at gains of 100. In real time, the board's 12-bit ADC takes 500k samples/sec on 16 channels (eight differential). The ETS capability results from using a custom, 20-MHz, system-timing ASIC, the DAQ-STC, which handles timing and ADC triggering. The IC contains 10 counter/timers: four are for the analog inputs; four are for the analog outputs. Users can access a 4-bit programmable frequency divider and two 24-bit general-purpose up-down counter/timers that have double-buffered inputs.



High-frequency acquisition is only one of the features that seem destined to raise users' expectations for data-acquisition boards in this price range. Although you've been able for several years to buy boards that perform all of their offset and gain trims via software, the AT-MIO-16E-2 is free not only of analog trims, but also of address jumpers and switches. It conforms to the ISA bus Plug-and-Play standard that Microsoft will implement in Windows 95. Until the new operating system becomes available, the board's vendor is shipping a configuration utility program with the board. A lower cost board, the $995 AT-MIO-16XE-50, also features Plug-and-Play configurability. This board, whose maximum A/D-conversion rate is 20k samples/sec, shares most of the features of the AT-MIO-16E-2—even its ability to accept 16 pseudo-differential inputs.

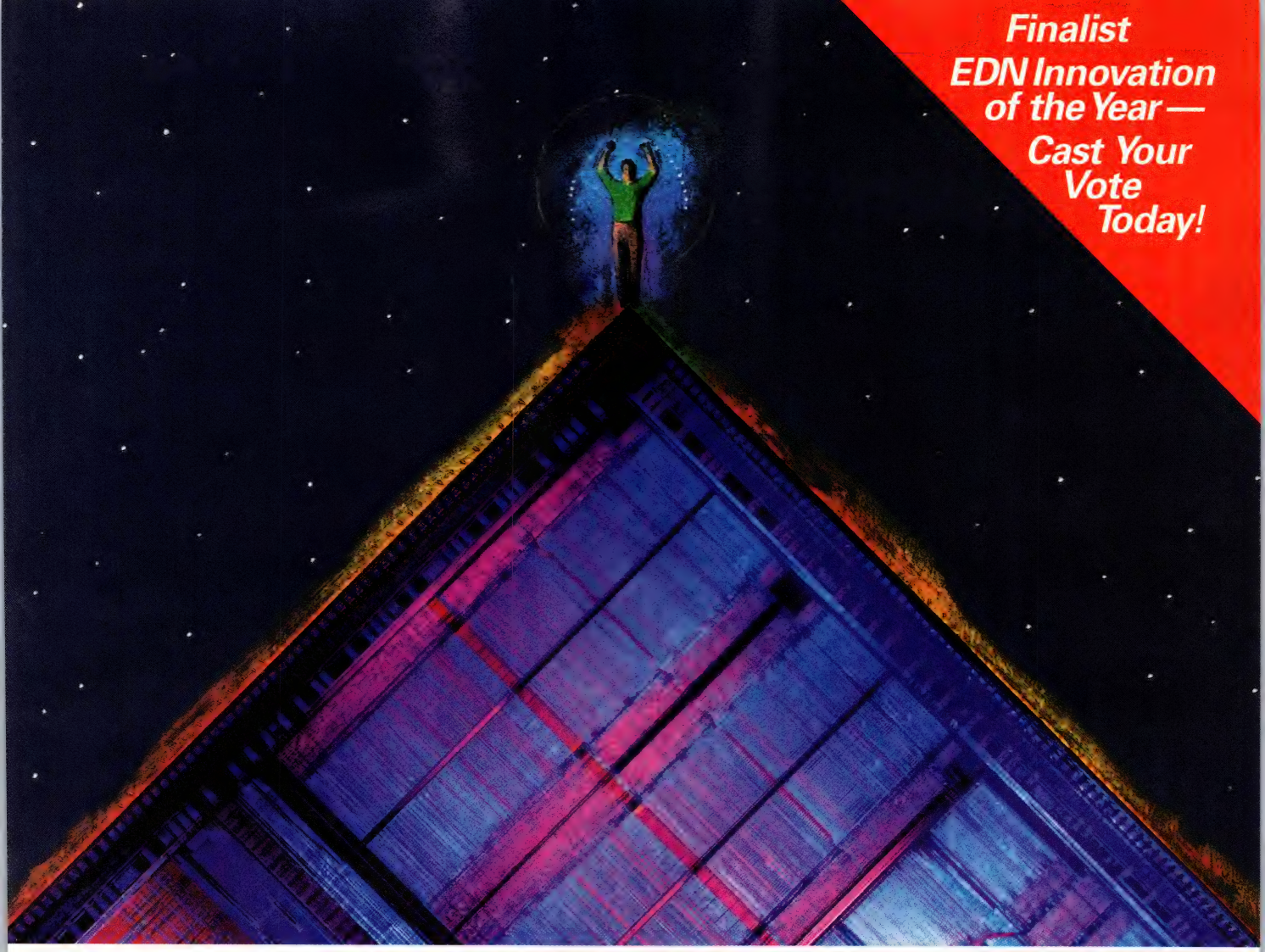
To vote for this entry as Test and Measurement Product of the Year, mark the appropriate box on the ballot.

NATIONAL INSTRUMENTS CORP
AUSTIN, TX
(512) 794-0100

MODEL 6517 ELECTROMETER

Keithley's Model 6517 electrometer measures currents from 10^{-16}A (100 atta-amperes, or aA) to 20 mA, resistances from 0.1 to $10^{16}\Omega$, charges from 10^{-15}C to 2 μC, and voltages from 1 μV to 200V. The 6½-digit-resolution unit can time-stamp its readings and can simultaneously display the external temperature and relative humidity—variables that are all-important to the interpretation of measurements of high resistances and low currents. A type K thermocouple senses temperatures from –190 to +1350°C. The meter includes cold-junction compensation for the thermocouple. The $4490, 10-lb, half-rack-width, portable instrument accepts plug-in scanners for multichannel measurements and includes a 5½-digit-resolution programmable voltage source that covers 5 mV to 1 kV in two ranges. Built-in mathematical functions calculate polynomials, percentages, per-

(Continued on pg 60)



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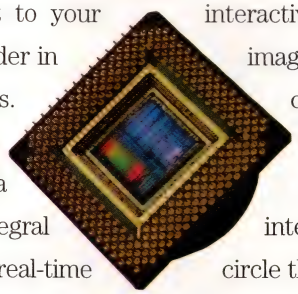

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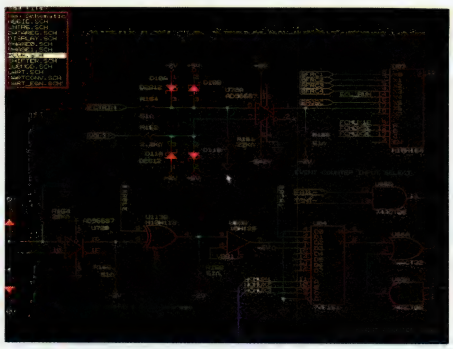

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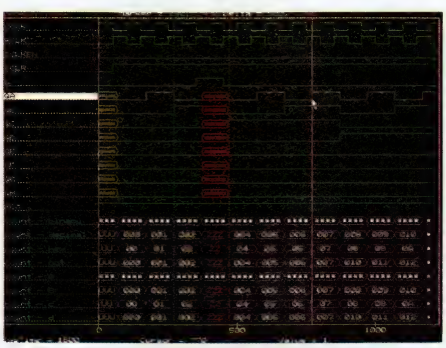

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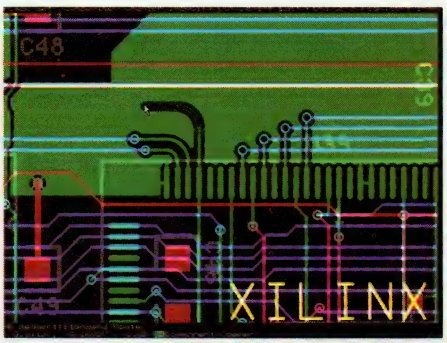

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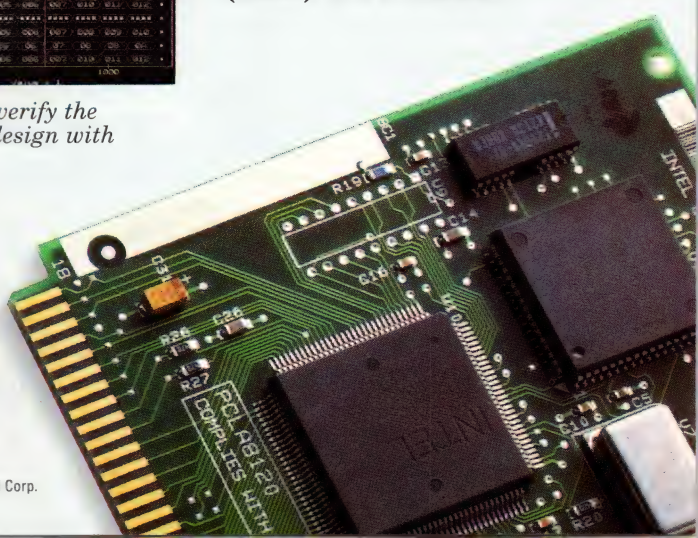

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CIRCLE NO. 122

TEST & MEASUREMENT *(Continued)*

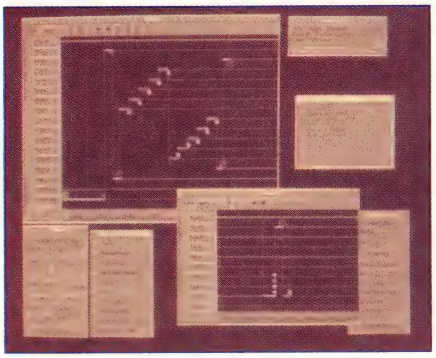
centage deviations, and ratios, and make base-10 logarithmic calculations.

Fast measurements of low currents and high resistances are unusual. (Remember that 10^{-16}A is only about 600 electrons/sec.) You should not infer from the top conversion speed of 125 readings/sec or the maximum IEEE-488 bus transfer speed of 2500 internally stored readings/sec that the instrument makes all measurements at such high speeds. Nevertheless, the unit is fast for a unit that measures such low currents and high resistances. The bandwidth from the input to the rear-panel preamp output is 100 kHz.

To vote for this entry as Test and Measurement Product of the Year, mark the appropriate box on the ballot.

KEITHLEY INSTRUMENTS INC
CLEVELAND, OH
(216) 248-0400

EMBEDDED SYSTEMS



WINDVIEW EMBEDDED-SYSTEM SOFTWARE

Unlike other debuggers that freeze an embedded system under development to take a single "snapshot" of system activity, WindView runs in real time without crashing the system. WindView helps embedded-software developers visualize the dynamic behavior of their embedded-system software.

The program takes advantage of debugger calls built into the maker's real-time operating system. This analytic and diagnostic program graphically presents the complex interactions between real-time tasks, interrupt-service routines, and system utilities on a remote workstation. The program can continuously record and time-stamp (to 1-μsec resolution) task state transitions, message passing, semaphore changes, and user-defined events. Engineers can halt or single-step one task in a multitasking system without affecting the other tasks' operation. WindView costs from $5000 (single qty) to $2500 (10+ qty).

To vote for this entrant as Embedded Systems Product of the Year, mark the appropriate box on the ballot.

WIND RIVER SYSTEMS INC
ALAMEDA, CA
(510) 748-4100

PSOSELECT RTOS KERNEL

A very compact real-time operating system (RTOS) kernel, pSOSelect requires only 1.8 kbytes of ROM and 320 bytes of RAM in its minimal form. It can expand, however, to a full implementation of pSOS+, the RTOS kernel on which it's based. You can use the kernel in embedded products that have stringent memory constraints or in more complex systems that require more OS resources. A configuration tool lets you choose the nature and quantity of capabilities you need—for example, four tasks, two semaphores, and a four-deep message queue.

The pSOSelect software consists of a compact core module and a set of the traditional pSOS+ operating-system objects. The core module contains the standard pSOS+ priority-based preemptive scheduler for creating and running tasks, as well as the standard i_return system call for interaction with interrupt-service routines. By adding other objects during configuration, you can create a pSOSelect environment with essentially unlimited OS services. Development licenses for pSOSelect cost from $4000.

To vote for this entrant as Embedded Systems Product of the Year, mark the appropriate box on the ballot.

INTEGRATED SYSTEMS INC
SANTA CLARA, CA
(408) 980-1500

DISKONCHIP FLASH-MEMORY MODULE

With DiskOnChip, a multichip flash-memory module, portable and embedded PCs can include "disk" storage that takes up no space. DiskOnChip replaces a computer's BIOS EPROM, storing a replacement BIOS and providing either 1 or 2 Mbytes of nonvolatile flash memory with a disk-emulation interface.

DiskOnChip is software compatible with DOS and pin compatible with BIOS EPROMs. To provide full read/write capability in a device that replaces a read-only BIOS ROM, DiskOnChip's controller intercepts disk-boot and BIOS calls and transfers control, as appropriate, to the replacement BIOS or to flash-file-system software. Together, the replacement BIOS and the flash software occupy about 100 kbytes of the flash memory, leaving the remainder available for storing programs or data. DiskOnChip is available in standard DIP and SMT packages. In quantities of 1000, the 1-Mbyte version costs $80, and the 2-Mbyte version costs $125.

To vote for this entrant as Embedded Systems Product of the Year, mark the appropriate box on the ballot.

M-SYSTEMS INC
SANTA CLARA, CA
(408) 654-5820

POWER SOURCES

PT6500 SERIES SWITCHING REGULATORS

The PT6500 Series switching regulators use a custom current-mode control IC that permits a 550-kHz switching rate. This high rate allows the use of small capacitors and magnetic components. The result is a small (0.36×1.64×1.16-in.) package size and high power density (38.6 W/in.^{3}). These 14-pin SIP (single inline package) converters come in three versions: The PT6501 provides a 5 to 3.3V conversion; the PT6502 converts 5 or 3.3V to a 1.5 to 2.5V range; and the PT6503 converts 5 to 2.5V. The PT6501 allows easy integration of devices, such as high-speed, low-voltage Pentium processors, into 5V systems without the need to redesign the central power supply. The PT6502 is a convenient source for the low terminating voltages required by BTL/Futurebus+, CTT, HP, and GTL buses.

(Continued on pg 65)

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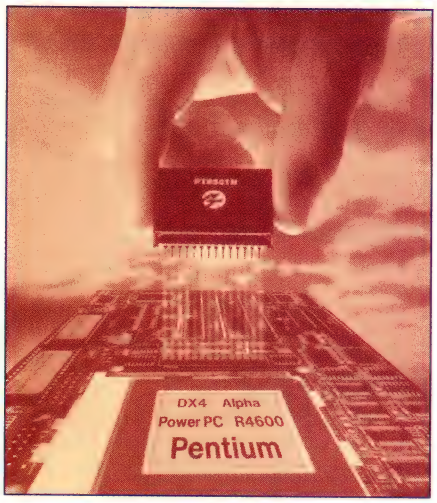
POWER SOURCES *(Continued)*



All models provide 8A maximum output current. All PT6500 converters can run at full-rated current with only free-air convection (40 to 60 linear feet/min air flow) at 60°C ambient. By adding an external resistive voltage divider, you can adjust the output voltages for all models over a wide range. Packaging options for the PT6500 Series allow vertical, horizontal, or surface mounting. Electrically isolated top or side heat tabs are available for heat-sink attachment. The junction-to-ambient thermal resistance (θ_{JA}) is 17°C/W. $25 (1000).

To vote for this entrant as Power Source Product of the Year, mark the appropriate box on the ballot.

POWER TRENDS INC
BATAVIA, IL
(708) 406-0900

3C050M POWERDEX LITHIUM BATTERY

The 3C050M Powerdex 3V lithium primary battery with 50-mAh capacity is only 0.7 mm thick, and thinner versions are in development. Powerdex batteries come in a coplanar, copper side-tab configuration that accommodates soldering or spot welding directly on a pc board. The 3V nominal voltage allows you to use only one battery instead of two alkaline cells, and the direct solder or weld connection eliminates the cost and space a battery holder would require. The 3×4-cm ultrathin batteries target "smart-card" applications, such as bank, phone, toll, asset-control, security, and RF-tag cards. The chemical components of the Powerdex Series are lithium-metal anodes, a highly conductive organic electrolyte, and high-purity manganese-dioxide cathodes.

These lithium batteries have a relatively flat discharge curve. If you divide the 50-mAh capacity by the load current in mA, you'll obtain the time in hours to the "knee," beyond which the

voltage drops rapidly. The 3V, 50-mAh 3C050M is the first catalog product in the ultrathin series. Custom versions, with different capacities, dimensions and thicknesses, are also available. For applications that don't demand the ultimate in thinness, other Powerdex 3 and 6V batteries offer higher capacity. The 3C050M costs $1.20 (50,000).

To vote for this entrant as Power Source Product of the Year, mark the appropriate box on the ballot.

GOULD INC
ELECTRONIC POWER SOURCES DIV
EASTLAKE, OH
(216) 953-5084

EDA

HDL-ICE ASIC EMULATION SYSTEM

The HDL-ICE ASIC emulation system merges programmable hardware emulation with hardware-description languages (HDLs) to let IC designers rapidly prototype designs created with Verilog or VHDL. The heart of this innovation is "synthesis-for-emulation" technology, which provides a faster method for mapping register-transfer-level (RTL) descriptions onto the field-programmable-gate-array (FPGA)-based emulation circuitry of the hardware emulator. Synthesis tools produce gate-level designs because that granularity level is ideal for describing gate arrays and cell-based ASICs. Earlier ASIC-emulation systems had to then map this gate-level description created by the logic synthesizer onto the more complex and less granular structures of the ASIC emulator's internal FPGAs. This two-step translation scheme was inefficient and time-consuming, and it lost the internal structure and signal layout of the original HDL description. Synthesis for emulation understands the unique logic resources of the FPGA-based emulator and directly makes a closer mapping between the HDL description and the emulation hardware. The net result is a 1000-times faster translation speed between HDL and emulation configuration.

Design starts with a system description written in an HDL. The HDL-ICE software converts this description into optimized logic equations and then maps these equations directly onto the 80 FPGAs comprising the system's hardware-emulation logic. The software also allows you to combine presynthesized and hand-optimized logic designs with the RTL descriptions. The HDL-ICE system can emulate designs to 250,000 gates and includes a 1152-channel logic analyzer with an eight-event, eight-state trigger.

To vote for this entrant as EDA Product of the Year, mark the appropriate box on the ballot.

QUICKTURN DESIGN SYSTEMS INC
MOUNTAIN VIEW, CA
(415) 967-3300

LOGIC ANIMATOR

The system includes rapid-prototyping software that partitions and maps a logic design into a timing-correct, gate-for-gate, and wire-for-wire configuration within an array of field-programmable gate arrays (FPGAs). These FPGAs reside on a single-board system with an emulation cable that supports as many a 448 bidirectional I/O pins. You use these I/O pins to interface with the target hardware, to feed internal nodes to a logic analyzer, or to drive ICs that will become part of the ASIC. The system accepts designs in a variety of standard netlist formats, including EDIF and Verilog. The software incorporates a clock-tree analyzer that identifies critical clock signals and partitions the logic accordingly. The software also allows you to place the portions of your design on critical paths into high-speed logic in the emulation hardware to maxi-

EDA (Continued)

mize the emulation speed, typically 8 to 16 MHz. You can also connect devices—memories, for example—to the Logic Animator, boosting the system's gate capacity and improving mapping efficiency.

The software costs $49,900, and the hardware-emulation box costs $39,000. Using this scheme, you can purchase several hardware boxes, download your design into them, and distribute the emulators to your development team. For example, you might want to have several emulators for the software-development team and another for board-level development. Once you download the design to the emulation boxes, you don't need the emulation software, so you need only one copy of the software for any number of emulation boxes.

To vote for this entrant as EDA Product of the Year, mark the appropriate box on the ballot.

QUICKTURN DESIGN SYSTEMS INC
MOUNTAIN VIEW, CA
(415) 967-3300

BEHAVIORAL COMPILER

This behavioral compiler automatically transforms behavioral specifications for data-intensive or control-oriented designs written in VHDL or Verilog into optimized gate-level netlists. The compiler requires no netlist for input; it works directly from the behavioral description. As a result, the compiler can reduce design time by 10 times and speed simulations by orders of magnitude. The software provides hardware allocation, data-path and memory-I/O scheduling, and controller inferencing. It supports a broad range of data-intensive algorithmic applications, such as telecommunications, memory controllers, multimedia, and data encryption.

To provide a high-quality implementation, the compiler uses exact, technology-dependent, bit-level timing and area information for all data-path elements. Although researchers have been working on behavioral synthesis for more than 15 years, this software package is the first to provide general-purpose support for data-path, control-oriented, and memory-I/O-dominated designs; direct runtime links to logic synthesis; technology-specific data-path elements (based on the company's technology-independent DesignWare building blocks); and support for both the VHDL and Verilog hardware-description languages. For scheduling, it supports multicycle, automatic chaining, and loop pipelining.

To vote for this entrant as EDA Product of the Year, mark the appropriate box on the ballot.

SYNOPSYS INC
MOUNTAIN VIEW, CA
(415) 962-5000

RESOLVE ANALOG OPTIMIZER

Using trial and error, you must juggle many variables, such as component values, operating temperature, and device geometries, to see how they affect analog-circuit performance. You must also juggle multiple performance criteria, such as speed, stability, and power dissipation. That's a lot of juggling to reach optimum circuit performance. The Resolve analog optimizer does all of this juggling for you. You specify a circuit topology and your design objectives; Resolve then systematically adjusts component values to meet your design objectives. The software is faster, more methodical, and usually more thorough than you could be. Engineers claim using the software yields a 10-times decrease in the time to solve complex analog-design problems. Resolve relieves you of the task of iteratively refining your design by hand: Once you get your design in the ballpark, Resolve zeroes in on optimum component values.

Analog optimization isn't new, but Resolve's ability to break a problem into tasks and distribute these tasks over a network of workstations is new. Without the ability to partition and distribute large problems, the computational complexity of analog optimization limits the technique to simple circuits. However, Resolve uses this ability to distribute the computational work, allowing optimizations for complex designs, such as switch-mode power supplies, to complete overnight instead of taking several days. Resolve optimizes circuits by combining two algorithms. The first is computationally intensive but can simultaneously evaluate many parameters over a wide range. The second algorithm is more efficient but has a limited range. The first algorithm gets the design to nearly optimum, and the second finishes the job.

To vote for this entrant as EDA Product of the Year, mark the appropriate box on the ballot.

CADENCE DESIGN SYSTEMS INC
SAN JOSE, CA
(408) 943-1234

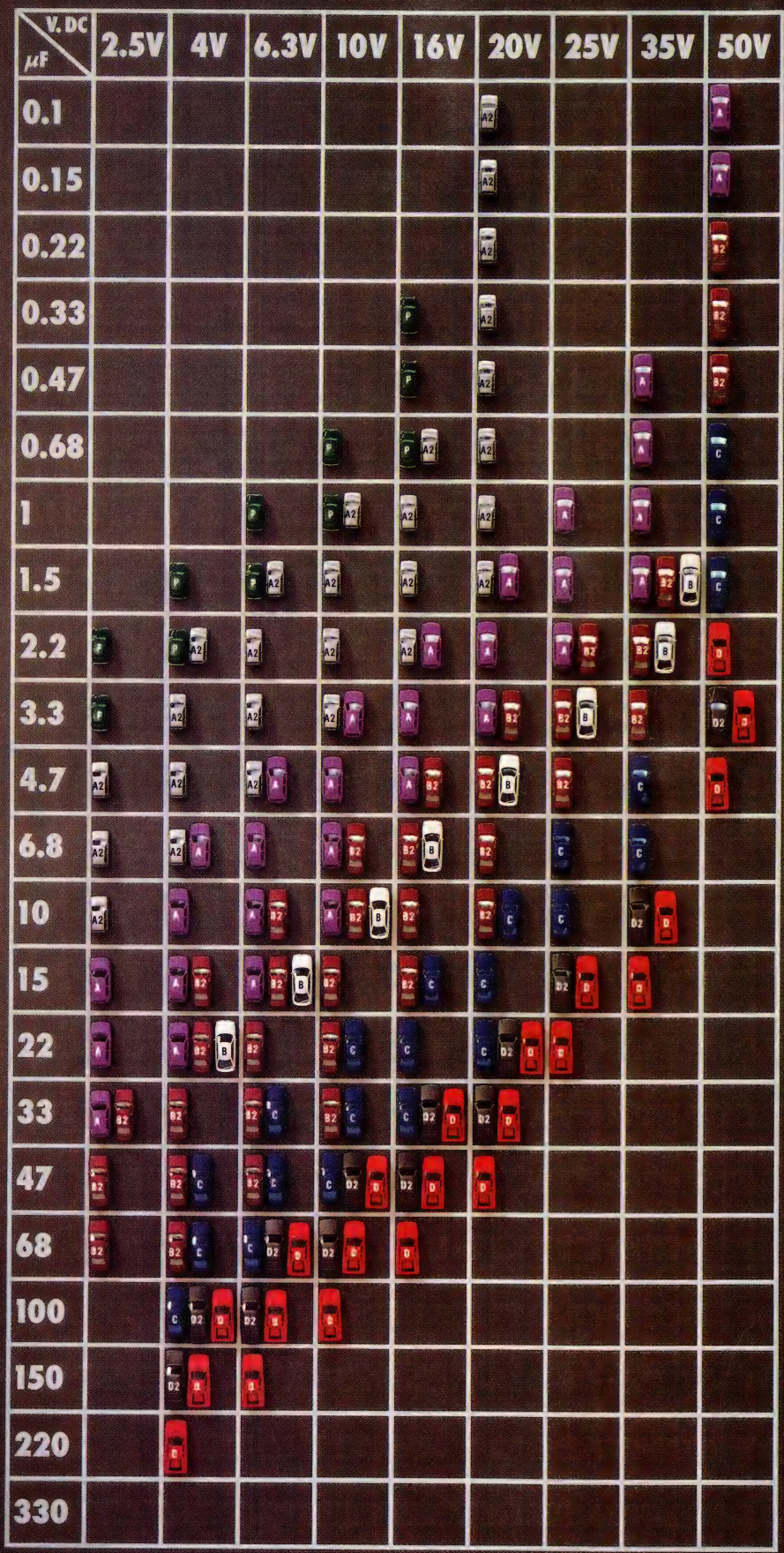
MISTRAL 2

The Mistral 2 behavioral-synthesis tool translates DSP algorithms written in data-flow language (DFL) into data-path architectures using fully synthesizable and scheduled register-transfer-level VHDL descriptions. It allows DSP-system designers to develop systems at a higher abstraction level and to focus on the critical global parameters of ASIC design, such as speed, area, and power consumption. Mistral 2 transforms a behavioral description of a DSP system into an architecture comprising execution units (ALUs, multipliers, address-calculation units, RAMs, and ROMs) and application-specific units that the system designer created. It also uses the behavioral description to perform the tedious task of scheduling hardware-resource sharing. From this architecture, Mistral 2 generates a structural description in VHDL or Verilog. You can use the resulting netlist to create gate-array, standard-cell, or full-custom ASICs.

Because it synthesizes architectures from both a behavioral description expressed in DFL and constraints, Mistral 2 allows you to rapidly explore alternative architectural implementations. DFL is the company's commercialized version of the Silage programming language developed at the University of California—Berkeley. You express constraints as "pragmas," which influence the number and type of execution units, define how resources are to be shared, assign variables to memory units, and schedule operations. These design "knobs" allow you to tweak your design for the desired result (speed, power consumption, area, and the like).

To vote for this entrant as EDA Product of the Year, mark the appropriate box on the ballot.

MENTOR GRAPHICS CORP
WILSONVILLE, OR
(503) 685-7000



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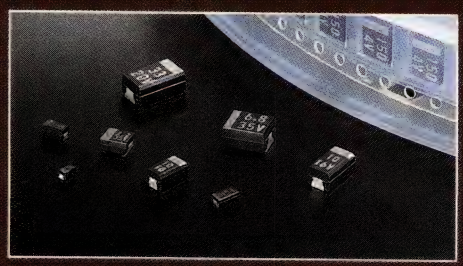
B	4.7	2.6	2.1
C	6.0	3.2	2.5
D2	5.8	4.6	3.2
D	7.3	4.3	2.8



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NEC

CIRCLE NO. 30

HDL-A

HDL-A is based on the work in progress to extend the VHDL hardware-description language (HDL) into mixed-signal design. Available since April 1994, HDL-A is the first language to demonstrate the viability of using VHDL extensions to describe analog behavior. The product combines the emerging IEEE 1076.1 specifications for the language extension and the company's experience with developing a proprietary analog hardware-description language called FAS. Unlike many HDLs, HDL-A is a compiled language that enjoys a 10- to 30-times performance advantage over other languages. Because it is based on VHDL, HDL-A is a top-down analog and mixed-signal system-design language that describes systems in multiple domains, including electrical, thermal, and mechanical, using one language. At the top level, you can use HDL-A to define and simulate a system using functional-block models. This way, you can assess a system's viability before creating a more detailed design. Complete, transistor-level simulations may be impractical for large systems, so the ability to define and simulate analog system components at a high abstraction level can greatly speed development.

HDL-A comprises a compiler, a runtime system, and a debugger. The package broadens VHDL's capabilities into the analog domain by implementing syntactic and semantic language extensions. HDL-A allows the use of implicit and explicit equations and adds dc and ac interpretation domains to VHDL's transient domain. Using HDL-A, you can designate a model's nature as electrical, mechanical, thermal, rotational, or fluid. Each "nature" has its own qualities, expressed as analog quantities. For example, you use the current and voltage quantities for models that have an electrical nature.

To vote for this entrant as EDA Product of the Year, mark the appropriate box on the ballot.

ANACAD ELECTRICAL ENGINEERING SOFTWARE
MILPITAS, CA
(408) 954-0600

LITE ENHANCEMENT TO TEST GENERATION

The low-impact testability-enhancement (LITE) tool, uses proprietary test-optimized algorithms to select and implement the most cost-effective test methodologies for an ASIC logic design. It allows you to use circuit transformations other than scan to improve your design's testability. In addition to inserting full- and partial-scan paths where they make sense, the package can employ nonscan design-for-test (DFT) techniques. The package takes advantage of predefined functional test vectors to guide it in the selection of a DFT technique. LITE can synthesize scannable-logic structures to create full- and partial-scan chains, LSSD, multiplexed scan, dual-clocked scan chains, IEEE 1149.1 boundary scan, and user-defined structures such as shadow scan.

To minimize the test logic's intrusion into your design, LITE employs fault grading to assess the testability effectiveness of any functional test vectors you supply. The package excludes from

scan-consideration logic that these functional vectors test, reducing the amount of test circuitry you need. LITE optimizes your design's testability without changing the timing of timing-critical paths. The tool selects and inserts ad hoc DFT techniques, such as control points and observability trees, and test registers. It also accommodates test structures, such as built-in self-test circuits that you define. LITE is part of the company's Sunrise testability and rules-checking tool (START) package.

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SUNRISE TEST SYSTEMS INC
SANTA CLARA, CA
(408) 980-7600

UNISOLVE CONCURRENT-ANALYSIS TOOL SUITE

The UniSolve concurrent-simulation and -analysis tool suite includes tools for electromagnetic compliance (EMC), analog- and digital-signal integrity, thermal analysis, and reliability analysis. These tools understand active device characteristics, physical interconnection structure, and substrate technology. Thus, you can apply the tools to the design of pc boards, multichip modules, and thick-film hybrid circuits. The tools individually analyze the various performance characteristics of a design. However, they share a common user interface, data base, and simulation models, so that you can see the effects of circuit changes simultaneously in all of the tools' simulation domains. For example, if you make a change to improve signal integrity, UniSolve lets you see the change's effect on the design's EMC profile. If you change a design's thermal characteristics by moving components on the substrate, UniSolve lets you see the change's effect on system reliability. Concurrent operation provides the linkage.

Each of the analysis tools employs empirically developed algorithms that provide quick, accurate results. Bell-Northern Research developed the various tools and empirical models of the UniSolve system over the past 12 years. You can define worst-case signal parameters for a boardful of components, for example, by making all signal traces appear to carry fast clock signals. The EMC module can then analyze all of the nets on the board in less than 1 sec. Color coding shows failing signals on the board design, allowing you to refine your signal definitions on only the traces that fail EMC specifications. You can further refine the model until you know the signal paths on which to focus. UniSolve requires no physical models. It can draw device characteristics from model libraries because it links to host CAD systems from Cadence, Mentor, Zuken-Redac, and other vendors with packages that support EDIF.

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UNICAD INC
WESTFORD, MA
(508) 692-8446

COMPUTERS & PERIPHERALS

SPRINTSCAN 35 HIGH-SPEED SLIDE SCANNER

The SprintScan 35 slide scanner digitizes high-resolution images in approximately 30 seconds—5 to 15 times as fast as comparably priced scanners. Proprietary sensor technology enables the device to scan high-quality images in one pass, rather than three. The scanner works with any Macintosh or Windows-based PC, and it scans any 35-mm transmissive media, including positives or negatives that are mounted, unmounted, or in strips.

The SprintScan 35 operates at resolutions as high as 2700 dpi. The device captures 10 bits each of red, green, and blue, measuring 1024 shades of each, for a total of more than one billion colors. It sends scanned images to a computer, via a SCSI-2 interface, at 24 bits per color—8 bits each for red, green, and blue. Onboard circuitry provides real-time sharpening and smoothing,

eliminating post-scan processing. The SprintScan 35 costs $2495.

To vote for this entrant as Computers and Peripherals Product of the Year, mark the appropriate box on the ballot.

POLAROID CORP
CAMBRIDGE, MA
(617) 386-2000

CARDIO-486 MOTHERBOARD

The Cardio-486 is a credit-card-sized, PC/AT-compatible motherboard, incorporating a 486 μP. The 3.37×2.13×0.22-in. board also contains a VGA controller, a floppy-disk controller, 8 Mbytes of RAM, serial and parallel I/O interfaces, and mouse and keyboard connections. Because of its small size, the board is suited for applications such as point-of-sale (POS) terminals, portable and handheld equipment, medical equipment, VCRs, fax machines, factory automation, and navigation equipment.

The board connects via the manufacturer's 236-pin card connector. It uses the latest chip-on-board (COB), tape automated bonding (TAB), and thin small-outline packaging (TSOP) techniques to conserve space. The board is available in 3.3 and 5V versions and costs $1000 (1000) with 8

Mbytes of RAM.

To vote for this entrant as Computers and Peripherals Product of the Year, mark the appropriate box on the ballot.

EPSON AMERICA INC
TORRANCE, CA
(310) 782-5174

COMPACTFLASH REMOVABLE MASS-STORAGE SYSTEM

CompactFlash, a mass-storage system based on flash memory, fits in electronic products that are even too small for PCMCIA cards. However, with a PCMCIA adapter, a CompactFlash module is also usable in a PCMCIA Type II slot. A module weighs about half an ounce and measures 36×43×3.3 mm. To simplify the use of CompactFlash, each module contains a disk-emulating ATA (ATbus-attachment) controller.

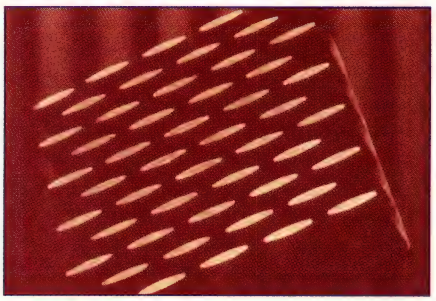
CompactFlash modules are available in capacities of 2, 4, 10, and 15 Mbytes. Corresponding OEM prices (quantities of 5000) are $75, $109, $200, and $250.

CompactFlash requires no batteries and uses less than 5% of the host-system power required by a disk drive because it's based on flash memory, according to the manufacturer. A module can tolerate 2000-g shocks while operating—higher than the tolerance of most products in which it is likely to be applied.

To vote for this entrant as Computers and Peripherals Product of the Year, mark the appropriate box on the ballot.

SUNDISK CORP
SANTA CLARA, CA
(408) 562-0500

COMPONENTS, HARDWARE & INTERCONNECTS



ELLIPTICAL PIN FIN AERODYNAMIC HEAT SINK

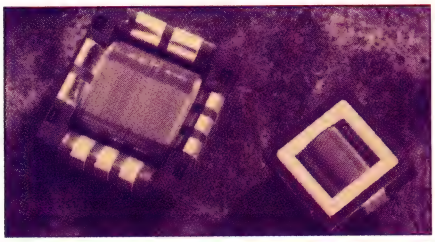
A heat sink designed for microprocessors uses elliptical-profile pin fins modeled after an airplane wing to reduce boundary-layer air buildup and vortex effects. Thus, the device minimizes downstream air heating and reduces pressure drop in electronic enclosures. The lower pressure drop allows for the

use of significantly lower speed fans than those needed with round pin fins. The manufacturer cites the case history of a 4-μP array. Vortex shedding created a prohibitive backpress with the use of heat sinks with round pin fins, which reduced downstream airflow and made cooling the fourth processor in the series impossible. From using the heat sink with elliptical pin fins, 90% of the air reached the fourth processor.

The cooling device uses an innovative manufacturing process. Previous casting methods were not capable of producing high enough cross-sectional aspect ratios. The new technique uses a vacuum applied to the die-cast cavity mold, which allows for the creation of thin component walls and high pin-fin aspect ratios. The method reduces the porosity that exists in nonvacuum die-cast parts. Low porosity means high material density and, thus, high thermal conductivity. $12.50 (5000).

To vote for this entrant as Components, Hardware, and Interconnects Product of the Year, mark the appropriate box on the ballot.

AAVID ENGINEERING INC
LACONIA, NH
(603) 528-3400



PGF SURFACE-MOUNT POWER MAGNETICS

The PGF (precision-geometry foil) family comprises high-power, high-frequency inductors and transformers for use in switch-mode power supplies. The PGF magnetics come in IC-style headers with wide "J" leads for mounting on high-current pc-board traces. Two available footprints occupy 0.59 and 1.25 $in.^2$ of board space. Devices with heights ranging from 0.3 to 0.5 in. handle power levels from 50 to 200W and currents to 40A dc. Power densities are typically 250 to 500W/$in.^3$ with operating frequencies from 200 to 400 kHz for single-ended forward converters; densities are greater for higher operating frequencies. Low-profile heat-sink designs contact the winding and core simultaneously for baseplate-cooled converters.

Innovative manufacturing techniques make the surface-mount magnetics possible. The PGF line complements planar, pot-core, and toroidal-core magnetics. Planar magnetics suffer from poor winding-to-heat-sink thermal conduction. Pot-core and toroidal magnetics use a winding conductor of thick foil, Litz wire, or round or rectangular wire, with less surface area than thin foil of equivalent circular mils. These have thermal shortcomings similar to those of planar magnetics.

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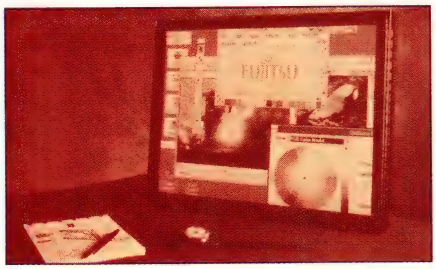
PULSE ENGINEERING INC
SAN DIEGO, CA
(619) 674-8100



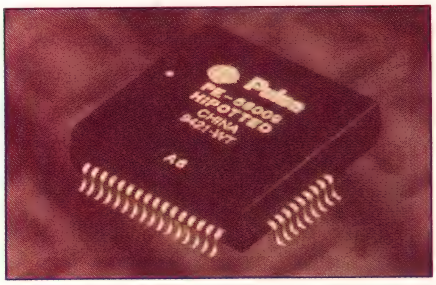
FPF21C8060UA PLASMA DISPLAY PANEL

The Model FPF21C8060UA-02 is a 21-in. (diagonal), ac-memory plasma unit that the manufacturer claims is the largest full-color flat-panel display in volume production. The display has 640×480-dot resolution, and its 6 bits (64 levels) of gray scale per pixel yields more than 260,000 colors. With the use of the appropriate interface board, the panel accommodates either digital RGB or NTSC video signals. Thus, the device can display VGA video or standard television transmissions. Overall package dimensions, including the integrated drive circuitry, are 18.9 in. high × 15.75 in. wide × 1.26 in. thick. The panel weighs less than 5 kg (11.2 lbs). A >140° viewing angle allows off-axis viewing without image distortion.

The display requires two power sources: 180V at an average current of 100 to 700 mA (depending on the image displayed) and a peak current of 4A and 5V at an average current of 1.9A. As a screen-saving and power-limiting measure, an automatic power-control function reduces brightness if the 180V supply's average current exceeds 550 mA. This current drain corresponds to a 40% display rate, meaning that 40% of the pixels are lit at their maximum brightness. CRT technology presently represents the only alternative for producing 21-in. screens. Active-matrix, thin-film-transistor LCDs offer full-color capability, but at a producible size limited to about 10 in. diagonally. Units at 21-in. exist only in prototype form. $10,000 in unit quantity.

To vote for this entrant as Components, Hardware, and Interconnects Product of the Year, mark the appropriate box on the ballot.

FUJITSU MICROELECTRONICS INC
ELECTRONIC COMPONENTS DIV
SAN JOSE, CA
(408) 922-9000



PE-68009 TRANSMISSION-LINE FILTER MODULE

The PE-68009 module provides filtering and waveshaping for transmitted or received data signals in local-area networks (LANs). The device incorporates pre-equalization elements that accommodate inexpensive, unshielded twisted pair, instead of coaxial cable. These elements, in tandem with passive low-pass filters, ensure that signals comply with IEEE network standards. The PE-68009 matches transmission-line impedance to that of the LAN controller or transceiver, and, thus, reduces signal reflections and noise on the line. The filter contains elements designed to filter and suppress conducted and radiated electromagnetic interference. The module provides electrical isolation between a network node and the transmission line.

The PE-68009 uses IC-style packaging: a square form factor, with leads on all four sides. High-volume transfer molding keeps encapsulation costs down, and a low-stress molding material has an 18- to 45-ppm coefficient of thermal expansion. Computer modeling reduces the size of magnetic components by 25 to 35%. Finally, a new nickel-zinc ferrite material used in common-mode chokes also reduces component size and offers improved EMI performance to boot. The result is a 1-in. square, surface-mountable module that weighs only 8.5 gm. $13.49 (100,000).

To vote for this entrant as Components, Hardware, and Interconnects Product of the Year, mark the appropriate box on the ballot.

PULSE ENGINEERING INC
SAN DIEGO, CA
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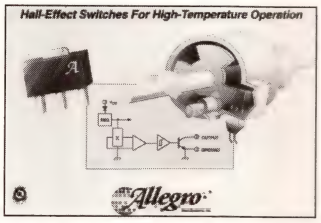
36-bit-wide bus logic for wide-bus applications. The Widebus+ SN74ABT-32xxx family of advanced bus logic has a 5-nsec propagation delay, provides –32- and +64-mA output drive, and is available in 80- or 100-pin plastic shrink QFPs. A bus-hold feature stores the last known state of the bus, avoiding the need for discrete pullup resistors. You can sue the transparent, bidirectional SN74ABT32245PZ data transceiver as four 9-bit, two 18-bit, or one 36-bit transceiver. $10.95 (1000). The 32543PZ 36-bit registered transceiver has two sets of D-type bidirectional latches for data storage. $12.10 (1000). Other family members include a 36-bit universal bus transceiver, a 16-bit, triport, universal-bus exchanger, and an 18-bit, triport, universal-bus exchanger. **Texas Instruments Inc**, Denver, CO. (800) 477-8924, ext 4500. **Circle No. 463**

Multimedia reference design provides an MPEG-compliant add-in board for <$100 in volume. The reference design for PC add-in cards extends the multimedia capability of a PC to play full-resolution, full-motion video and CD-stereo sound. The design uses TI's TMS320AV220 video-CD MPEG-1 decoder, TI's TMS320AV120 MPEG audio decoder, and AuraVision's VxP201 video-playback processor. The three ICs form the core of the full-motion, video-playback board, featuring an ISA bus interface, support for up to 1280×1024-pixel resolution, interpolated zoom, and full color control. The design kits include a suite of driver software licensed by AuraVision to complement the hardware design for Windows 3.x and DOS. The design kit includes an evaluation board, schematics, a parts list, pc-board layout, software, and documentation for $3000. **AuraVision**, Fremont, CA. (510) 252-6800. **Circle No. 464**



Hall-effect switches offer high-temperature operation. The A3121-A3123 and A3141-A3144 Hall-effect switches are available in temperature ranges of –40 to +150°C. The switches operate from 4.5 to 24V dc and have open-collector outputs that sink up to 25 mA. The versions offer operating sensitivities from 100 to 350 gauss and hysteresis levels of 55 to 105 gauss. From $1.04 (1000). **Allegro MicroSystems Inc**, Worcester, MA. (508) 853-5000.
Circle No. 465

3.3V FPGAs suit portable-computing applications. Devices from the company's ACT1 and ACT3 family are available in 3.3V versions. The 1200-gate A10V10B and the 2000-gate A10V20B are from the ACT1 family. The ACT3 family includes devices with 1500 to 10,000 gates. The company is also offering new packaging options, including the 1-mm-thick VQFP package for FPGAs (field-programmable gate arrays) with up to 4000 gates. The TQFP is available for 4000- to 6000-gate devices and meets the specifications for Type II and Type III PCMCIA cards. The 10,000-gate part comes in a 313-lead ball-grid array. ACT1 devices start at $7 for the A10V10B, and ACT3

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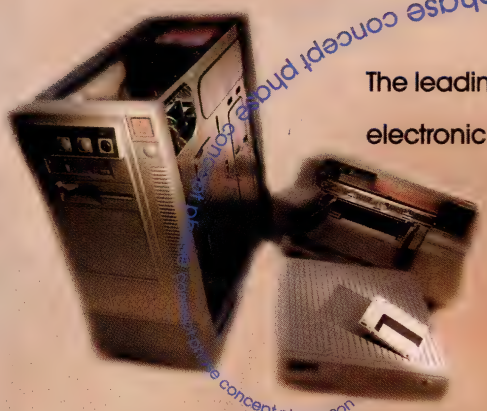

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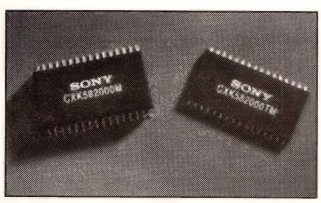
devices start at $17.70 (OEM) for the 1500-gate A14V15A. **Actel Corp**, Sunnyvale, CA. (408) 739-1010.
Circle No. 466

Stackable 3-D flash-memory module provides up to 128 Mbits of high-density storage. Commercial flash-memory modules range from 16 ($213 (100)) to 128 Mbits ($1638 (100)). Military modules range from $261 (100) to $2019 (100). The stacking modules permit placing more memory per square inch of board space than with nonstacking memory. SRAM modules are also available. **DensePac Microsystems**, Garden Grove, CA. (714) 898-0007.
Circle No. 467



2-Mbit SRAM has 85-nsec access time and is pin-compatible with 1-Mbit RAMs. The CXK58200 is a 256k×8-bit CMOS SRAM with an 8-μA standby current and a 4.8-μA data-retention current at 40°C. A version with an 85-nsec access time costs $40, and a 100-nsec version costs $30. **Sony Electronics Inc**, San Jose, CA. (800) 288-7669.
Circle No. 468

DAA chip set provides 6-kV isolation for fax/modem cards. The K² data-access-arrangement (DAA) chip set connects to a telephone line tip and ring signals. The set includes an eight-pin SOIC, a 16-pin QSOP, and a 20-pin QSOP. The three chips are 1.4 mm high and mount inside fax/modems, including PCMCIA cards. The chips accommodate 300- to 28.8k-bps V.34 data rates and provide off-hook relay control, ring-indication output, internal two- to four-wire conversion, voice/data control, and caller ID. The chips operate from 3.3 or 5V and have a 30-mW active power consumption and a 10-mW standby power consumption. Protection circuitry meets FCC Part 68, DOC CS-03 European isolation standards, and UL 1459 requirements for hazardous voltage and leakage. $8.50 (10,000). **Krypton Isolation Inc**, Fremont, CA. (510) 713-9100.
Circle No. 469

16- and 32-Mbit mask ROMs operate below 3V with 150-nsec access time. The mask ROMs operate from 2.7 to 3.6V supplies, dissipating 35 mA while operating and 30 μA in standby mode. The devices come in 44-pin SOP and 48-pin TSOP packages. The 16-Mbit LH53V16500 costs $20 (100), and the 32-Mbit LH53V32500 costs $30 (100). **Sharp Electronics Corp**, Camas, WA. (206) 834-2500. **Circle No. 470**

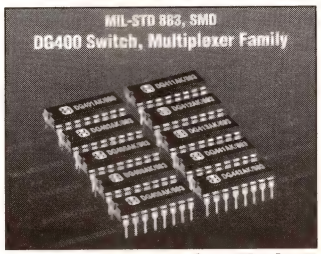
4- and 16-Mbit DRAMs offer extended data output for 25-nsec page-cycle times. The 1M×4-bit HM514405C extended-data-output DRAM has a 1k/16-msec refresh; 60-, 70-, or 80-nsec row-address access times; and 25-, 30-, and 35-nsec row-address access times for a continuous burst of address retrieves. A device with the 60-nsec row-address access time and 25-nsec address-access cycle time costs $22 (1000). The 1M×16-bit HM5116165A DRAM has a 4k/64-msec refresh and costs $110 (1000) for the 60-nsec row-access and 25-nsec address-access cycle-time version. **Hitachi America Ltd, Semiconductor and IC division**, Brisbane, CA. (800) 285-1601, ext 11.
Circle No. 471

V.32bis modem chip set for Windows PCs costs $29. The HSM192DW controllerless modem chip set uses the system host CPU (386, 486, or Pentium) to perform modem microcontroller software functions, such as AT commands, data compression, and error correction. This approach eliminates the need for a modem controller chip, RAM, and ROM. The change saves board space, power consumption, and cost, according to the vendor. The chip set works with Microsoft's Windows architecture, the standard Windows communications driver, and virtually any communications or fax applications for Windows. The chip set supports data rates and fax speeds up to 19.2k bps, the AT Command Set, V.42 and MNP4 error correction, and V.42bis and MNP5 data compression. The HSM192PW chip set supports the PCMCIA standard and costs $31 (100,000). **AT&T Microelectronics**, Allentown, PA. (800) 372-2447.

Circle No. 472

Op amp offers high-voltage, 2A output-current capability. The OPA544 operates from ±10 to ±35V supplies and has a slew rate of 8 V/μsec. The device drives electromechanical device, including motors, valves, and speakers. It also suits programmable power supplies and magnetic deflection-coil drivers. Other features include a 100-pA input-bias current, internal current limit, and internal thermal-shutdown protection when junction temperature reaches approximately 165°C. The device operates from –40 to +85°C. Housed in a five-pin TO-220 package, the device costs $6.95 (100). **Burr-Brown Corp**, Tucson, AZ. (602) 746-1111.

Circle No. 473



Analog-switch family has MIL-STD-883 and standard-microcircuit-drawing (SMD) number classifications. The DG400 analog-switch family includes 10 devices that operate from –55 to +125°C. Prices range from $7.44 (100) to $18.29 (100). **Harris Semiconductor**, Melbourne, FL. (800) 442-7747, ext 7290. **Circle No. 474**

Low-power wireless prescalers for personal communication services. The PMB 2313 prescaler for mobile-radio devices up to 1.1 GHz suits battery-powered systems, such as cellular phones, cordless telephones, and wireless LANs. The low-power device operates from voltages as low as 2.7V and offers a standby mode. The PMB 2314 is for similar applications up to frequencies of 2.1 GHz and offers 2.7V operation. Each costs $2.61 (1000). **Siemens Components Inc, Integrated Circuits Division**, Cupertino, CA. (408) 777-4500.

Circle No. 475

Arrays of MOSFET power transistors provide fast switching and eliminate voltage-level shifting. The Power+monolithic arrays have a 5V logic-level

interface, eliminating the need for predrive voltage-shifting circuitry. The power-transistor arrays provide switching speeds to drive fractional horsepower motors in high-frequency applications. Arrays of three, four, or six power DMOS transistors are available. Typical on-resistance is 0.4Ω, and peak current is 3A/channel. Voltage rating is 60V. From $1.37 (1000). **Texas Instruments Inc**, Denver, CO. (800) 477-8924, ext 4500. **Circle No. 476**

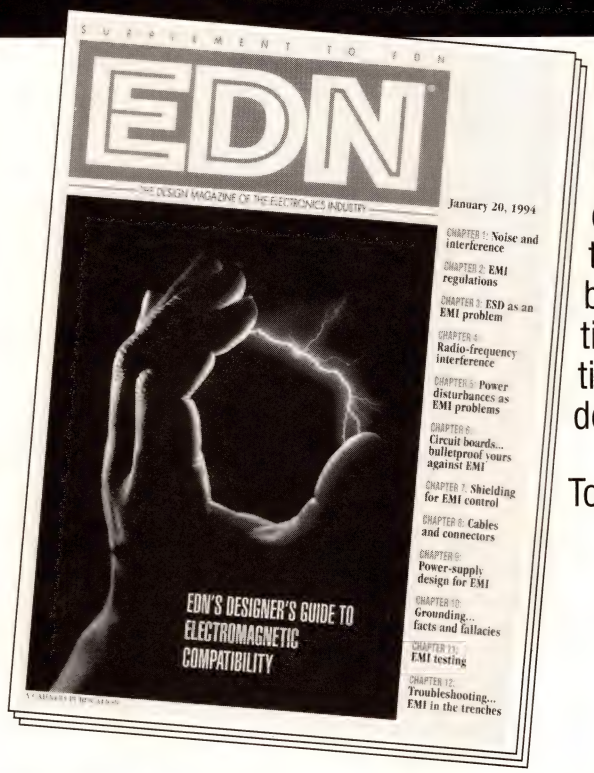
12-bit, 20M-sample/sec ADCs offer low distortion. The TTL-compatible AD9022 and the ECL-compatible AD9023 have a spurious-free dynamic range of 75 dB at 1 MHz and 74 dB at 9.6 MHz. The converters have an analog input bandwidth of 100 MHz, well beyond the Nyquist limit for the devices, suiting them to direct intermediate frequency to digital conversion or undersampling. The dynamic nonlinearity is <0.5 dB, and the S/N ratio is typically 65 dB. The devices provide a track-and-hold amplifier, a reference, and control logic and timing. Both parts require +5V and –5.2V. Typical power dissipation is 1.3W. Available in 28-pin ceramic DIP and surface-mount packages, they cost $140 (1000). **Analog Devices Inc**, Wilmington, MA. (617) 937-1428. **Circle No. 477**

Addressable scan-port device extends boundary-scan testing to system level. The SN54/74ABT8996 addressable scan-port device permits the testing of boards in a system using IEEE 1149.1 boundary-scan chip- and board-level test patterns without reformatting. The device acts as a serially addressable switch that directly interfaces primary test-access-port (TAP) signals to secondary TAP signals. Instead of requiring each board in a system to have its own dedicated test-mode line on the backplane, the device lets up to 1021 boards share one multidrop test mode line. $6 (1000). **Texas Instruments Inc**, Denver, CO. (800) 477-8924, ext 4500. **Circle No. 478**

486 PC chip sets for Microsoft's Chicago operating system are plug-and-play-compatible. According to the company, the chip sets reduce product-design cycles by combining all the building blocks for a complete plug-and-play-compatible, green PC. The chips include the CS4040 system controller $14 (10,000); the CS4041 system controller $17 (10,000); the CS4745 I/O IPC $21 (10,000); and the FS84049 Peripheral Component Interconnect enabler $10 (10,000). **Chips and Technology Inc**, San Jose, CA. (408) 434-0600. **Circle No. 479**

QAM digital-transmission receiver for cable TV increases channel capacity. The single-chip BCM3100 QAMLink, a 64/256-quadrature-amplitude-modulation (QAM) digital-transmission receiver, suits cable-TV applications. In the 256-QAM mode, it achieves 40-Mbps digital-transmission speeds. According to the company, the chip increases the chan-

A NONTRADITIONAL APPROACH TO EMI



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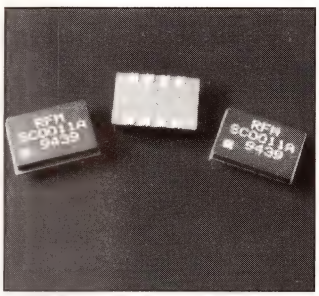
nel capacity of coaxial cable by a factor of 10 to 25. The chip integrates QAM demodulation, Nyquist filtering, carrier and timing synchronization, and adaptive equalization. The IC comes in an 80-pin PQFP and costs $50 (1000). **Broadcom Corp**, Los Angeles, CA. (310) 443-4490. **Circle No. 480**

EEPROM for video-monitor plug-and-play applications. The 24LC21 1-kbit EEPROM meets the Video Electronics Standards Association (VESA) Data Display Channel (DDC) specification for plug-and-play operation between PCs and video monitors. The device holds all the monitor specifications a graphics controller needs to automatically configure the controller for the monitor. The device comes in an eight-pin SOIC or DIP, draws 1 mA in operation, and costs $0.92 in volume. **Microchip Technology Inc**, Chandler, AZ. (602) 786-7200. **Circle No. 481**

Hall-effect gear-tooth sensors operate down to zero speed. The A3046, A3056, and A3058 Hall-effect sensors are monolithic ICs that switch in response to differential magnetic fields that ferrous targets create. When you combine the devices with a back-biasing magnet, the sensors can provide a 50% duty cycle or switch on the leading or trailing edge, or both, of a passing gear tooth or slot. Each device contains two quadratic Hall-effect sensing elements, a voltage regulator, temperature-compensating circuitry, a low-level amplifier, a Schmitt trigger, and an open-collector output driver. The sensors operate over wide temperature ranges, making them suitable for industrial and automotive applications, such as antilock braking and ignition timing. From $1.94 (1000). **Allegro MicroSystems Inc**, Worcester, MA. (508) 853-5000. **Circle No. 482**



Surface-mount clocks offer 300- to 700-MHz frequency. The SC00xx family of digital clocks provides better power-supply noise immunity and less jitter than do conventional ECL or PLL clocks, according to the maker. The differential sine-wave clocks feature a worst-case symmetry of 48 to 52%, a typical period jitter of 15 psec p-p, and a maximum jitter of 30 psec p-p. From $13.50 (1000). **RF Monolithics Inc**, Dallas, TX. (214) 233-2903. **Circle No. 483**

1-Mbit SRAM in surface-mount package. The M624256 is a 256k×4-bit SRAM in 17-, 20-, or 25-nsec speeds. The device comes in a 0.400-in.-wide, 28-pin SOJ package. Prices range from $26 to $39 (1000), depending on speed. **SGS-Thomson Microelectronics**, Lincoln, MA. (617) 259-0300. **Circle No. 484**

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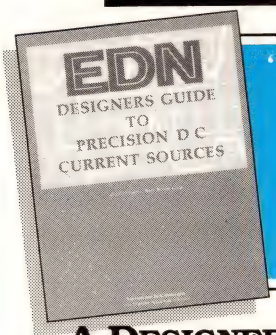

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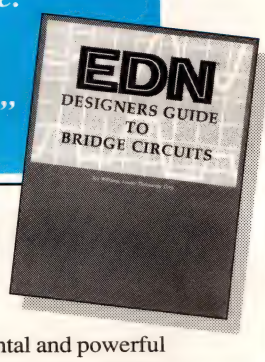

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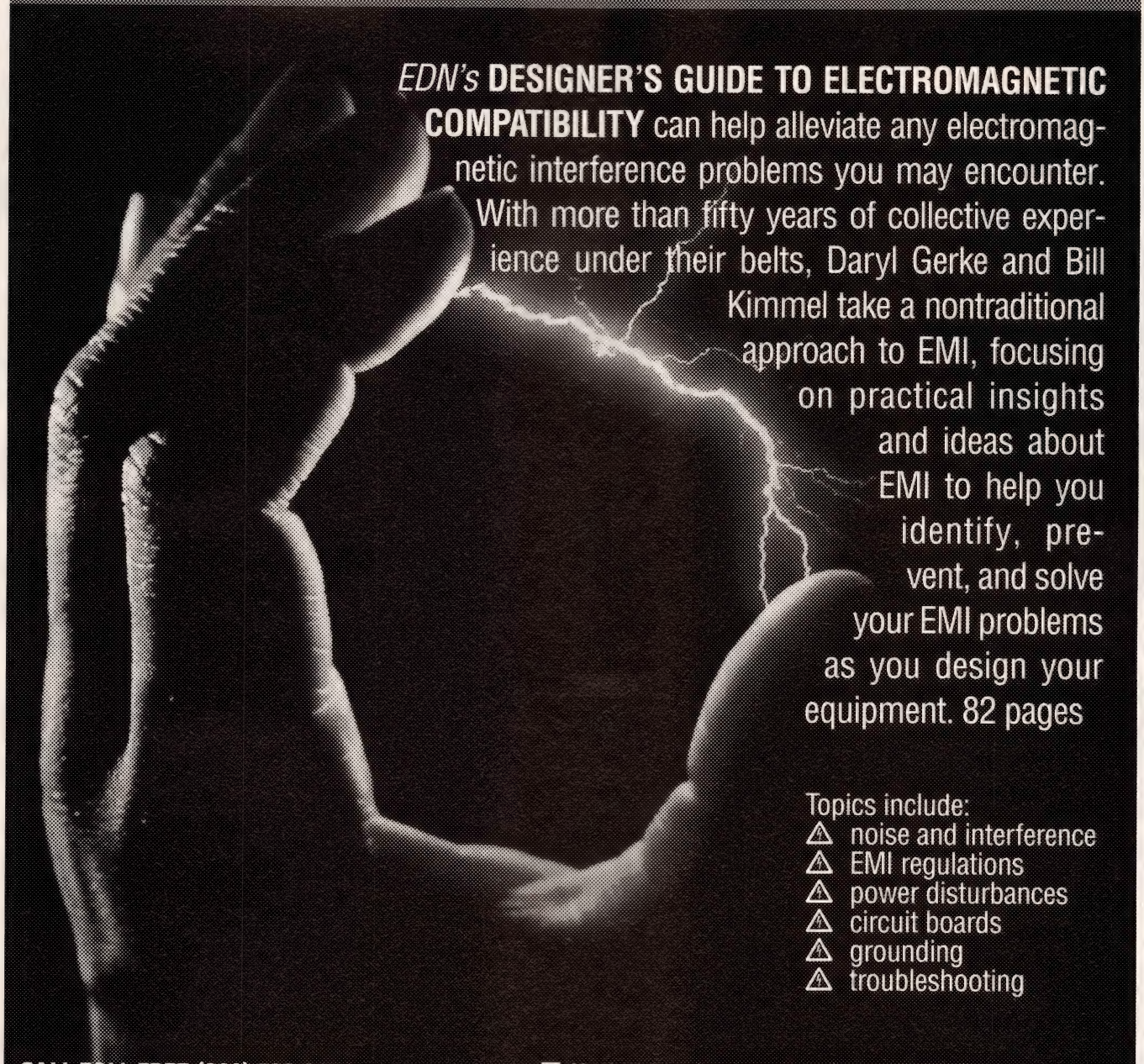

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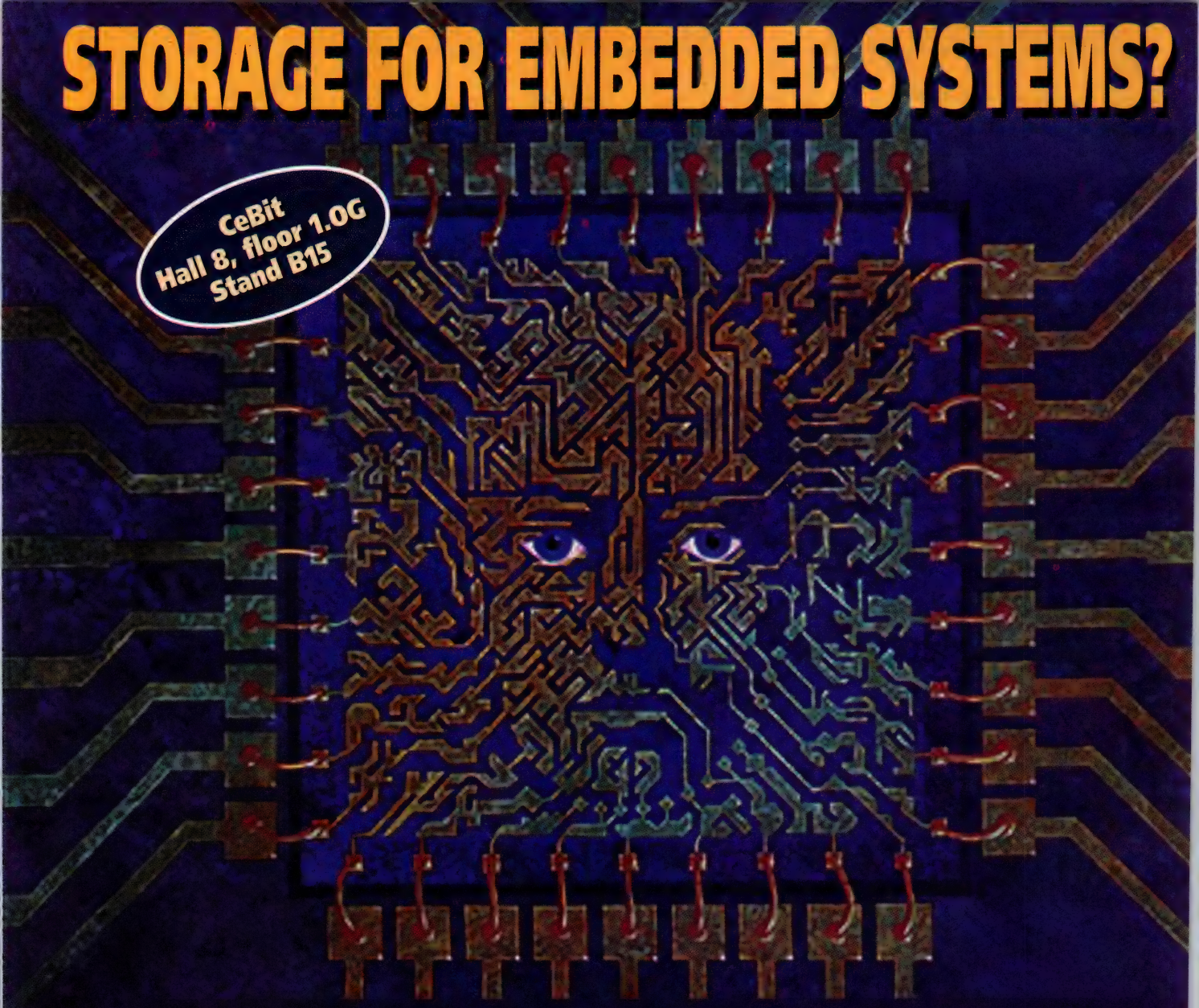

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BRIDGE CHIPS HELP CONNECT HOST AND EXPANSION BUSES TO THE PCI BUS

JOHN GALLANT, TECHNICAL EDITOR

The PCI bus is filling the need for a high-performance local bus to accommodate the increasing bandwidths of new designs. Now, many vendors are offering bridge chips to help PCI get on and off the buses of various CPUs.

It is difficult to pick up a trade journal on computing design or embedded systems and not find a mention of the Peripheral Component Interconnect (PCI) bus. PCI is rapidly becoming the local bus of choice for new computer designs, and its industrywide acceptance promises high-volume and low-cost PCI peripherals at the right performance levels. The driving force for this growth is the need for bridge chips, which connect various CPUs to the bus and connect the bus to a variety of system-expansion buses.

PCI's high bandwidth of 132 Mbytes/sec for 32-bit transfers and 264 Mbytes/sec for 64-bit transfers allows the bus to support high-speed transactions for multimedia and embedded applications. Because the PCI bus is a mezzanine bus, it requires bridge chips to

The Viper chip set from Opti comes in desktop and laptop versions. The chip set connects a 3.3V Pentium μP and provides main-memory and cache controllers.

LOOKING AHEAD

With multimedia, CD-ROM, and audio standard features of PCs, the need for a high-performance local bus is growing each year. Plug and play, extending to devices on the motherboard, is becoming a requirement, and video conferencing and the use of on-line services are expanding rapidly. Additionally, Windows 95 with its multitasking capabilities will place more performance demands on the system.

The features of the PCI bus fit the bill for most of these demands. These features include multiple-bus mastering, processor independence, configuration registers for plug-and-play operation, and very high bandwidth. The PCI Special Interest Group is considering a proposal to increase the bus's data-transfer rate to 66 MHz, which would provide a bandwidth of 528 Mbytes/sec for 64-bit transfers.

You can expect to see more bridge chips for a variety of host- and expansion-bus architectures. Texas Instruments plans to soon introduce two more PCMCIA-to-PCI bridges that will interface two 16-bit PC Cards or 32-bit CardBuses to the PCI bus.

accommodate the protocols of various CPUs and host buses. The CPU-independent PCI bus supports both CISC and RISC μPs, and bridge chips are available for the Advanced Micro Devices Am29000; the Digital Equipment Corp Alpha; the Intel Pentium, i960, and i486; the Mips 4000; and the Motorola PowerPC μPs. Chips are also available for bridging the PCI bus to the ISA, EISA, VME, VL, and PCMCIA buses. In addition, PCI-to-PCI bridge

TABLE 1—PCI-BRIDGE CHIPS

Vendor	Part no.	Bridge type	No. of chips	Price	Features
Chips & Technologies Inc Circle No. 326	F84049 PCI enabler	PCI to VL-bus	One	$10	Converts standard VL-bus signals to PCI bus signals; write buffers boost performance and make flexible timing parameters; supports as many as four PCI bus masters
Digital Equipment Corp Circle No. 328	21050	PCI to PCI	One	$28.70 (5000)	One interface connects to the primary PCI bus, and the other connects to a secondary PCI bus; allows concurrent transactions on both interfaces at 132 Mbytes/sec; programmable rotating-arbitration function supports six secondary bus masters; provides read prefetching for memory-read transactions; provides as many as 8 words of write posting for memory-write transactions
IBM Microelectronics Circle No. 329	IBM27-82351	PCI-to-PCI bridge	One	$21.50 (1000)	Attaches to the primary PCI bus through one of its two interfaces; second interface provides connection to a secondary PCI bus, which allows multiple expansion slots; operates at 33 MHz and has a 32-bit address and data bus; 160-pin PQFP
Intel Corp Circle No. 330	82430NX (Neptune)	Pentium to PCI and PCI to ISA or EISA bus	Two or three	ISA version, $80.30; EISA version, $107.25 (10,000)	Contains an integrated PCI, cache, and main-memory bus controller, integrates SRAM for address tagging; handles 512 kbytes of burst-mode cache SRAM; memory controller handles 2 to 512 Mbytes of main memory; single-chip bridge to ISA bus, two-chip bridge to EISA bus
	82430FX (Triton)	Pentium to PCI and PCI to ISA bus	Four	$41.95 (10,000)	Comprises the Triton system component, two identical Triton data-path units,and the PCI ISA/IDE accelerator; provides an alternative to native signal-processing DSP, which uses 100-Mbyte/sec PCI-to-DRAM data streaming; third-generation chip set aimed at 75, 90, and 100 MHz; contains a PCI bus-master IDE controller; handles 4 to 128 Mbytes of main memory; supports 256 or 512 kbytes of second-level cache
Mentor Arc Inc Circle No. 331	Winset-PCI-Pentium	Pentium to PCI and PCI to ISA bus	Three or four	$75 (sampling)	Comprises the 86C257 cache-memory and PCI-control unit, the 86C226 PCI-to-ISA bridge unit, and the 86C229 or86C239 data-path unit; controls as much as 256 Mbytes of main memory; PCI arbiter handles three PCI masters; power management complies with APM specification for energy (green) PCs; supports 64-kbyte to 1-Mbyte caches
	Winset-PCI-R4x00	Mips R4x00 μPs	Three	$75 (sampling)	Comprises the 64C257 cache-memory, and PCI-control unit; the 64C226 PCI-to-ISA bridge unit; and the 64C229 or 64C239 data-path unit. Write-back cache controller supports 1 Mbyte of cache; memory controller supports 256 Mbytes of main memory; power management complies with the APM specification
Motorola Inc Circle No. 332	MPC105	PowerPC to PCI	One	$62 (1000)	μP interface is a 32-bit address bus and configurable 64- or 32-bit data bus; write-through or -back cache controller supports as much as 4 Gbytes of cache memory; memory controller supports 256 Mbytes of RAM and 16 Mbytes of ROM; supports nap, doze, and sleep power-management modes; PCI interface acts as a master and slave device; PCI interface operates from 20 to 33 MHz

chips are available to expand the capabilities of the PCI bus.

A group of more than 300 companies, the PCI Special Interest Group, controls the PCI bus, now an open specification in its second revision. The revision specifies that the bus operates at a maximum 33 MHz rate and has a 32-bit address/data path. The specification also allows for multiple bus masters that arbitrate for control of the PCI bus. Bridge chips must match the byte

TABLE 1—PCI-BRIDGE CHIPS (CONTINUED)

Vendor	Part no.	Bridge type	No. of chips	Price	Features
Newbridge Microsystems Circle No. 333	Universe	PCI to VMEbus	One	$160 (1000)	FIFO buffer decouples the VME bus from the PCI bus to handle block transfers; handles little- and big-endian translation in software; FIFO buffer decouples the interrupter from the interrupt handler
Oki Semiconductor Circle No. 334	PCI Megacell	i486-like bus to PCI	One	$10,000	Contains a 32-bit PCI and 32-bit i486-like interface; two 4×32-bit address-, data-, and byte-enable-write FIFO buffers; supports master and slave modes; handles burst write-mode operations; PCI bus interface performs byte swapping; programmable address registers respond to accesses on its primary bus if the address falls into the range of those registers
Opti Inc Circle No. 335	Viper	Pentium to PCI bus and PCI bus to ISA bus	Three	Desktop version, $30; notebook version, $40 (10,000)	Comprises the 82C556 data-buffer controller, the 82C5557 system controller, and the 82C558N integrated peripherals controller; versions for desktop and notebook computers; notebook version includes power management; works with Pentium-class µPs from AMD (K5) and Cyrix (M1); memory controller handles 256 kbytes to 16 Mbytes of page-mode DRAM; operates from 3 and 5V Pentiums; employs level-1 cache in write-back mode
PLX Technology Inc Circle No. 337	PCI 9000 series	i960 to PCI	One (four family members)	9060, $46; 9036, 9060ES, 9060SD, $25	9060 has two DMA controllers with bi-directional FIFO buffers for each channel; FIFO buffers enable high burst rate on the local and PCI buses; eight 32-bit mailbox registers and two 32-bit doorbell registers; generates interrupts from several sources; in direct master mode, the device can generate type 0 and 1 PCI configuration cycles; other devices in family have lower feature set and lower cost
SIS Microelectronics Inc Circle No. 338	SPCIB	29K family of RISC µPs to PCI	One	$25 (10,000)	Internal 256-byte dual-port RAM (FIFO) buffers direct DMA and cross-bus transfers; host and PCI bus have separate clocks and operate independently; atomic transfer occurs because the device establishes simultaneous ownership of both buses during operation. Because FIFO is a dual-port RAM, filling and emptying of data can occur simultaneously
Texas Instruments Inc Circle No. 339	PCI1050	PCMCIA slot to PCI	One	$12 to $15	Interfaces two PC Card (PCMCIA) slots to the PCI bus; internal signal buffers allow hot insertion and removal of PC Cards; core logic and PCI interface operate from 5V, and the card interfaces can handle any combination of 3.3 and 5V PC Cards; register-compatible with the Intel 82365SL-DF ExCA controller; can be cascaded to handle as many as eight PC Cards
Toshiba America Electronic Components Inc Circle No. 340	Mako PCI chip set	Mips R4x00 series of RISC µPs to PCI	Three	$75 (1000)	Comprises an address-control chip and two identical data-path control chips; asynchronous PCI bus operation as fast as 67 MHz; PCI-to-ISA bus controls four PCI bus masters; handles one to eight banks of DRAM with a maximum of 256 Mbytes; controls as much as 1 Mbyte of second-level cache; the µP and cache operate at 3.3V, and the main memory and PCI interfaces operate at 5V

PCI-BRIDGE CHIPS

lanes of the PCI bus to the byte lanes of the host or secondary bus to which the PCI bus connects.

The primary function of a bridge chip is to map the address space of one bus into the address space of another bus, so that every bus master in a system sees the same address map. PCI provides three independent physical-address spaces: memory, I/O, and configuration. Configuration space is unique to PCI. A host bridge must support the minimum set of configuration-space registers, which allow for plug-and-play operation.

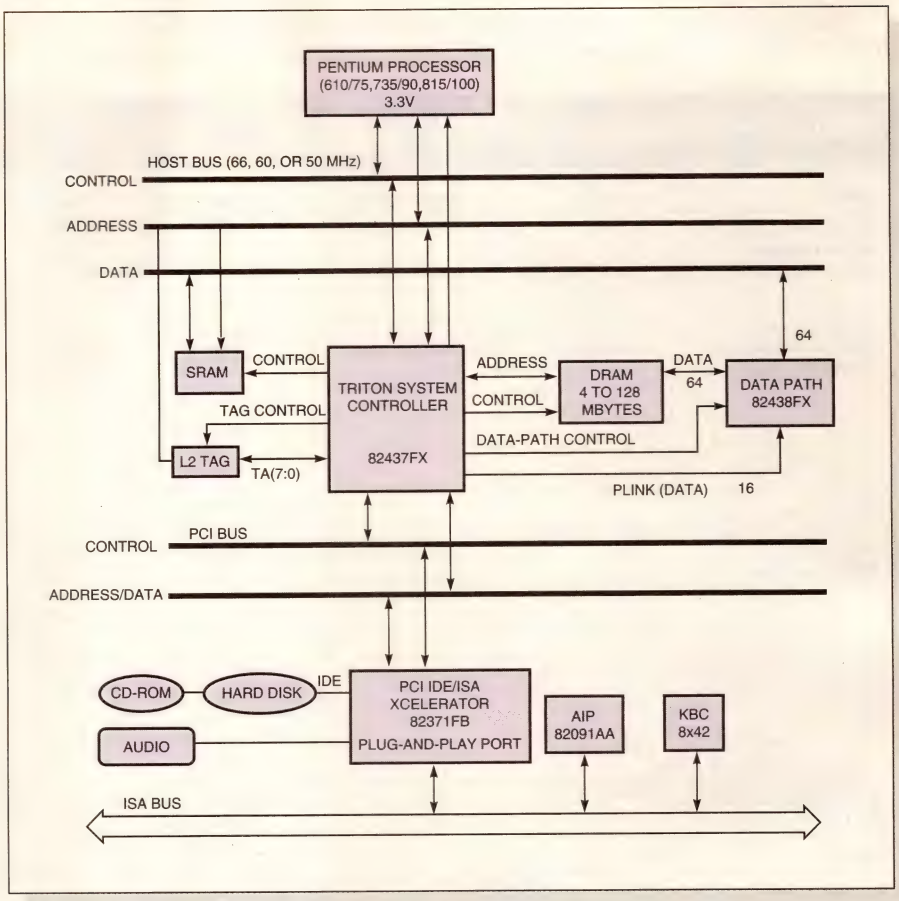
The bridge must match byte-ordering of its primary and secondary buses, which may involve byte-swapping between byte lanes. Some μPs may expect data on a different byte lane from the natural byte lane for that address for certain byte or word sizes. If so, the bridge chip must move data to the proper byte lane for that bus. To perform byte-swapping, the bridge must know the transfer size, which is not encoded in the address lines; instead, the bridge determines the transfer size from the byte-enable lines.

The preferred method of decoupling the PCI bus from the host or secondary bus is through the use of bidirectional FIFO buffers. Because the primary means of data transfer on the PCI bus is a burst, FIFO buffers let each bus keep pace with asynchronous data transfers. A bridge can include two types of buffers: write posting and read prefetch. Either bus can implement either type of buffer.

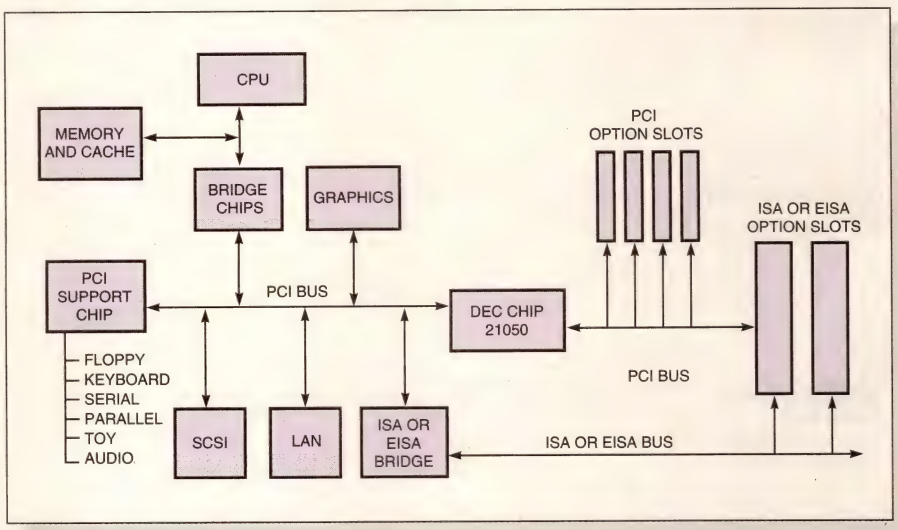
Write-posting buffers accept write data from one bus and acknowledge reception to that bus, freeing the bus to perform other transactions. The bridge temporarily stores or posts the write data until it can be written to the other bus. Read-prefetch buffers take the address from a read access and then read additional data. The bridge then holds that data in the buffer until a read access uses it, or until it is unusable.

Interrupts cause latency

The bridge chips must also handle system interrupts. When a system interrupt occurs, one device in the sys-



Intel's Triton is the third generation of chip sets that connects the Pentium and ISA bus to the PCI bus. Native signal processing uses 100-Mbyte/sec PCI data streaming.



Digital Equipment's DECchip 21050 PCI-to-PCI bridge chip expands a single PCI slot into multiple PCI card slots and allows for concurrent primary and secondary operations.

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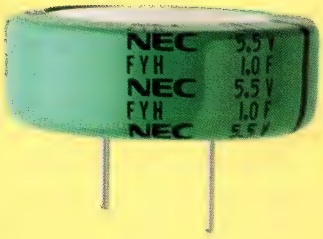

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tem can inform another device of an event that has just happened. By inserting wait states, the bridge chip intercepts and delays system interrupts while the system is flushing the buffers. The chips handle accesses across the bridge by maintaining the order of writes in both directions.

The bridge chips in **Table 1** use these techniques to connect a host or secondary bus to the PCI bus. Some chip sets, such as those from Intel, Opti, and Mentor Arc, contain main-memory and cache controllers for the appropriate µPs. These bridge chips, for desktop and laptop applications, include a separate chip that connects the PCI bus to a secondary ISA or EISA bus.

Bridge chips for the embedded market, such as those from PLX 22Technology and SIS Microelectronics, connect the Intel i960 and AMD 29000 RISC µPs, respectively, to the PCI bus. The PCI bus is finding its way into a variety of embedded applications, including printers, adapter boards, and backplanes for hubs and routers.

Many embedded applications do not contain a BIOS, so the µP must configure the system during power-up. For example, Cyclone Microsystems' i960-based intelligent I/O processor card uses the PLX Technology PCI 9060 bridge chip to connect to an on-card PCI mezzanine bus.

For industrial-control applications, Newbridge Microsystems offers the Universe chip, which bridges the VMEbus to the PCI bus. In 64-bit mode, the PCI bus transfers data more than three times faster than the theoretical limit of the VMEbus. Universe lets the VME industry take advantage of the new spectrum of high-end, low-cost PCI chips and for PCI vendors to take advantage of the large and diverse market for embedded-control applications.

The PCI-to-PCI bridge offerings from DEC and IBM extend the capabilities of the PCI bus, and DEC even includes an integrated PCI interface directly on the DECchip 21066 Alpha AXP µP. The PCI-to-PCI bridge chips expand the PCI bus limits beyond its maximum specified load limit of 10. Each connector on the bus represents two to three loads, so the specification recommends only three connectors per bus. Placing a PCI-to-PCI bridge chip in one of the slots lets you add slots to the base system.

However, according to Sassan Teymouri, engineering director at Adaptec, PCI-to-PCI bridge chips can cause problems with the BIOS. On power-up, the BIOS recognizes a bridge chip only in the primary slot of the PCI bus but not devices in the secondary slots. The BIOS companies are aware of this problem and are working to correct it. EDN

You can reach Technical Editor John Gallant at (617) 558-4666; fax (617) 558-4470.

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MINIATURE HARD DISKS SLIP DATA AND PROGRAMS INTO YOUR POCKET

CHARLES H SMALL, SENIOR TECHNICAL EDITOR

RIVALING the exquisite, miniature beauty of the Fabergé eggs made for the Russian czars, Personal Computer Memory Card International Association (PCMCIA) hard disks are tiny jewels crowning the hard-disk industry. Amazingly, disk makers squeezed the guts of a conventional, multiplatter hard disk into a 2.12×3.37×0.41-in. (approximately 54×85.6×10.5-mm), Type III PCMCIA package. Even thinner Type II hard disks also exist. (PCMCIA recently changed the official name for PCMCIA cards to "PC Cards.")

Weighing 3 oz or less, the Type III disks store an astounding amount of data—as much as 420 Mbytes. Be careful, though. Some makers quote storage for *compressed* files. If you detect this dodge, simply divide the quoted capacity by two to derive the real capacity.

Makers are producing these marvels with some oddball markets in mind besides the disks' obvious use in laptop computers. These markets include personal digital assistants (PDAs), electronic games, dedicated word processors, and automotive information and navigation systems.

MiniStor Peripherals Corp's PC Card hard disk employs a positive mechanical latch to lock its head actuator in place when the disk is not in operation.

Mobile computing is passé; *transportable* computing is in. If you work on a computer, you can now store your entire office on a slim, pocket-sized hard disk.

This list shows that disk makers are better engineers than they are soothsayers. PDAs failed in the market because potential customers could not figure out what the PDAs were or why anyone would want to buy one. This mystery persists to this day. Electronic games and dedicated word processors are price sensitive. PC Card hard disks cost as much as or more than these products themselves. However, PC Card hard disks *are* rugged enough to survive the automotive environment. Currently, a rental-car company is testing in-car navigation systems that use PC Card hard disks. Whether such systems will replace gas-station maps and the American Automobile Association's hand-customized route maps, only time will tell.

Everyone now on board

PCMCIA has done an excellent job of ensuring that designers have usable, workable standards. Because of PCMCIA's efforts, users can mix and match PC Cards from

all makers and can simply plug the cards into any device and expect them to work without problems or conflict. All PC Card hard disks comply with the PCMCIA's ATbus-attachment (as in IBM PC/AT) specification. So, all PC Card hard disks will be compatible with all PCs, both new and old.

Although some PC Card disk makers at first resisted the PC Card 3.0 Standard's requirement for a card-information structure (CIS), all PC Card hard disks now have a CIS. The host computer can interrogate any PC Card's CIS to determine the card's functions—such as low-voltage operation or DMA—storage format, and software drivers. This information is necessary for disks to comply with the Plug-and-Play Standard. All PC Card hard disks are plug-and-play and "hot-swappable," which means you can plug them in and out with the power on and without rebooting.

Maxtor's PC Card hard disks use a piezoelectric-film accelerometer to sense mechanical shocks. The piezoelectric shock sensor trips at shock levels that are only 10% of the shock, which would knock the head off track.

System software

As for software drivers for PC Card hard disks, PC Card hard-disk makers are sticking to the standard operating systems (OSs) for PCs: Microsoft Windows, OS/2, and the Macintosh OS. Drivers for workstation OSs are noticeably absent.

All PC Card hard disks require the host computer to have card-and-socket services software. SystemSoft's CardSoft PCMCIA device drivers are the most common, and Versa Technology also offers a package, called CCMSTR.SYS. PC Card hard-disk makers report that the software for their disks consumes 20 to 100 Mbytes of RAM.

Card-and-socket services software is not the only software you get with PC Card hard disks. Allowing for the worst case, Epson's $699 260-Mbyte PC Card hard disks come with a data-recovery program ominously named "DRoP."

Calluna formats its 260-Mbyte Type III disks at its factory in Scotland so that the user doesn't have to format them. The company's disks also have built-in, user-programmable software for data security and power management. The proprietary data-security software protects stored data with a password.

As storage devices, PC Card hard disks could hardly be more straightforward. You first run a setup program to install the device drivers. From then on, you simply plug the disk in and use it, just as you would any other drive. But the engineering that makes this smooth and simple perfor-

STACKING PC CARD HARD DISKS AGAINST SOLID-STATE FLASH MEMORY

Flash memory is an interesting alternative to rotating memory for many PC Card applications. Being solid-state, flash memory is more rugged than rotating memory. But flash memory is more expensive, costing $15 to $20 per megabyte (**Table 1**).

For example, SunDisk's PC Card flash memories meet the ATbus-attachment Standard, just as rotating memories do. These flash memories withstand 1000g shocks, either when the memories are operational or nonoperational. Most PC Card hard disks withstand 200 to 300g shock when operating and 500 to 1000 when not operating. Flash-memory access time is immediate vs rotating memory's 5- to 18-msec delays. For equal amounts of storage, flash memory consumes less current than does rotating memory, depending on number of reads and writes.

Flash memory is silent, whereas rotating memories emit 25 to 35 dBA of noise. Stop/start specifications that limit some rotating memories to 50,000 operations do not apply to solid-state devices. Flash memory fits in the 5-mm-thick Type I PC Card package vs the hard drives' thicker Type III packages. Further, SunDisk notes that data-transfer times can increase as rotating memories and some large-sector flash memories get crowded.

TABLE 1—PC CARD FLASH-MEMORY PRICING

Capacity (Mbytes)	Retail end-user street prices	OEM prices
1	$140 to $150	
1.8	$179 to $199	
2.5	$239 to $259	$75
5	$359 to $399	$109
10	$549 to $599	$200
20	$929 to $999	$250
40	$1399 to $1499	

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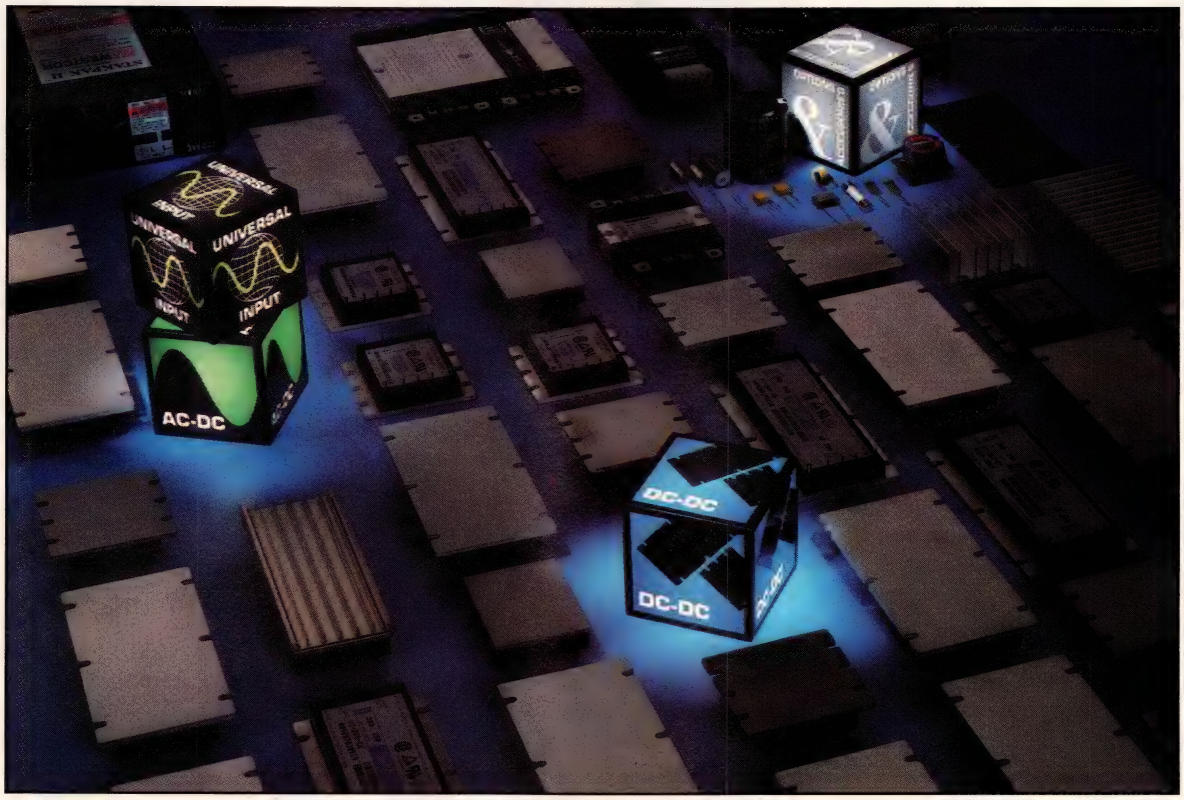

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mance possible is anything but straightforward.

The petite platters of PC Card hard disks are rotating so fast, and their magnetic domains are crammed so tightly together that the industry had to upgrade the read-channel electronics of higher capacity disks. At today's read-channel bit rates, the chances of less-than-perfect bits are much higher than with older, bigger, slower disks. All PC Card hard-disk makers have adopted partial-response, maximum-likelihood (PRML) decoding of bit streams of their higher capacity disks. PRML detects and corrects errors in these bit streams on the fly.

Alone among the dizzying swarm of new PC Cards, PC Card hard disks have electromechanical as well as electronic components. In general, electromechanical components are significantly less reliable than electronic components. In particular, a major manufacturer of redundant arrays of inexpensive disks (RAIDs) reports that the calculated MTBF that hard-disk manufacturers quote in their spec sheets are optimistic when compared to actual field experience. In contrast, MTBF for electronic equipment (using either Bellcore or MIL-SPEC methods) yields conservative figures compared to actual field-failure rates. (*EDN* is attempting to get permission to publish this disk research for publication in an upcoming article on disk technology.)

The disk industry is obviously concerned about these Lilliputian disks' ruggedness and resistance to shock and vibration. The disk makers expect users to bump, drop, and handle these precision devices with all the caution and dexterity customarily lavished on a $2 floppy disk. Today's PC Card hard disks can withstand as much as 200g shock during operation and up to 1000g when not in use. For reference, 200 and 1000g shocks are roughly equivalent to 4- and 8-ft drops, respectively, upon a medium-hard surface.

Shock deterring, clean running

Makers have achieved these goals via different routes. For example, MiniStor Peripherals Corp's $499 260-Mbyte disk employs a positive mechanical latch to lock its head actuator in place when the disk is not in operation. Once engaged, the latch requires no further force. In contrast, some PC Card hard disks use an energy-consuming magnetic lock that is less positive than the mechanical latch.

Intégral's PC Card hard disks park their heads off the platters, allowing the disk to resist shock. Further, because the heads never wear the media down by physically touching the platters, the disks provide unlimited power cycling.

The company characterizes its heads as "nanosliders" to signify that they are smaller and lighter than the "microsliders" that its larger disks use. These nanosliders have inherently lower mass and less inertia than the heads of larger drives, providing better shock resistance and fewer head crashers. Small heads allow for more tracks and higher storage densities. Smaller heads are also shorter than larger heads, permitting closer stacking of media platters.

MiniStor's PC Card hard disks' oversized spindle-motor bearing is the same component the company uses in its 3.5-in. disks. The large bearing protects the motor from shock.

Although some companies' disks admit filtered air to their head-disk assemblies (HDAs), MiniStor seals its HDAs and backfills them with dry nitrogen gas. The sealed unit should prevent dirt from fouling the disks' extremely tight mechanical clearances and allow the disks to operate at altitudes up to 40,000 ft.

PC Card hard-disk makers could not offset their platters down around their motors similar to the way automobile tire rims are offset back around their brake assemblies. To do so would reduce the already-minuscule writable area of the platters. Further, PC Card hard-disk makers often use glass platters, which tend to be perfectly flat, to enhance shock and vibration resistance. Consequently, the disk's spindle motors have to be especially thin. For example, Maxtor's new motor for its $595 (OEM evaluation units) PC Card hard disk measures 0.5 in. in diameter and is only 5 mil thick. The motor uses plain bearings instead of ball bearings to reduce the motor's size and to increase its strength.

Maxtor hasn't limited innovations to the disks' mechanical components. The disks use a piezoelectric-film accelerometer to sense and withstand mechanical shocks up to 2000g. Shocks can jar the head, causing it to skip to a wrong track during reads and writes. The shock sensor trips at shock levels that are only 10% of the shock that would knock the head off track. Once tripped, the disk suspends read/write operations, retaining the data in a buffer, until the shock stops. After the shock, the disk automatically writes the data.

Servos get stiffer

Like many manufacturers, MiniStor had to "stiffen" and "embed" its disks' servo systems. A "stiff" servo is a digital servo having a high sampling rate. The servo rate is simply a function of the number of servo-reference patterns per revolutions recorded on the platters and the platters' rotational speed. A

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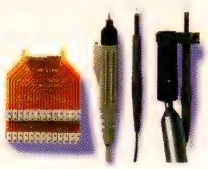

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high sampling rate provides tight control of the heads' actuators, keeping heads on track even if the going gets bumpy.

An embedded servo is an alternative to using one complete platter surface for servo information. Instead, all surfaces have bursts of servo data separated by data fields. This scheme allows disk designers to strike the required balance between capacity and ruggedness for each application. Another advantage of embedded servos is that they are less vulnerable to thermally induced misalignment of mechanical components because each head tracks its own servo burst.

Many paths to miniaturization

Intégral's PC Card hard disks look like other PC Cards on the outside but have fundamentally different insides. The company employs what it calls "dynamic head loading," which removes the heads from the disk when the power is off or when the disk is in standby mode. Other makers continue to use a downsized version of the "start/stop contact" method. In this method, the heads come to rest—perhaps in designated landing zones—on the platters' surfaces when the platters spin down.

Intégral says that, by parking its heads off the platters, the disks resist shock better than start/stop-contact disks do. Further, because the heads never wear the media down by physically touching the platters, the disks are capable of unlimited power cycling. In addition, because the heads are not resting on the platters at the instant the

LOOKING AHEAD

PC Cards are not just for portable computers anymore. The ever-growing swarm of PCMCIA cards is addressing every conceivable function: Rumors abound of a PCMCIA-compatible automatic ice-cube maker. The cards are just too handy for desktop-PC users to ignore.

You can expect new desktop PCs to increasingly sprout PCMCIA slots. And a host of suppliers makes inexpensive PC Card drives that you can retrofit either permanently or temporarily to your PC. Notable makers of PC Card hard-disk "drives" are Qtronix, Union Genius Computer Co Ltd, and Versa.

DataFab offers a $75 adapter, called Mobile Disk, for PC Card hard disks. You can plug the adapter into a PC's enhanced parallel port without rebooting your PC. Thus, you can access your PC Card hard disks from a desktop PC without opening the PC and installing a receptacle for the disk, which the industry confusingly calls a "drive." The adapter automatically configures itself for your PC's parallel port; the adapter then optimizes its data-transfer rate to suit the port. With the adapter, the maker supplies an optional soft carrying bag that also holds five PC Card hard disks.

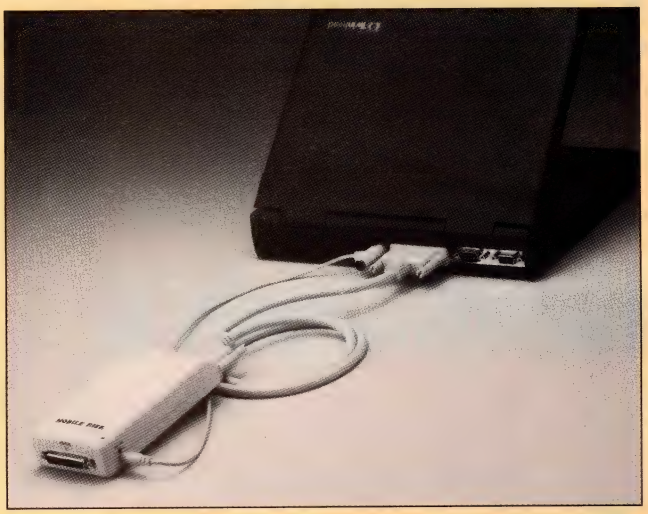
Other adapters, such as those from Pacific Rim Systems, mate conventional 3.5-in. hard disks to PCMCIA slots via a cable and a dummy PC Card. These adapters offer yet another way to enhance mass storage.

The success of PC Cards could cut into the sales of the portable computers for which they were designed. If you have your applications, files, and operating system on a PCMCIA hard disk, you can carry your office in your pocket. You can then set up shop anywhere you can plug in your tiny hard disk and boot up.

Even if you don't travel, you may find yourself needing a removable hard disk. Full-sized removable hard disks, or "cartridge" disks, have found a niche in graphics shops in which workers pop removable hard-disk cartridges into and out of their PCs the way others use floppy disks. The reason? Huge graphics files often don't fit on floppy disks.

PC Card hard disks can nearly match the capacity of cartridge disks and will certainly be less expensive. So, if multimedia and the Information Superhighway live up to their hype, we all may soon need PC Card hard disks so that we can handle the coming deluge of data raining down upon us.

In fact, you can already get a PC Card cartridge disk. SyQuest's SQ1080 sports a removable 2×2-in. cartridge disk that fits into a Type III PC Card. The cartridge holds 80 Mbytes and withstands 2000g shock. A PC Card and cartridge cost $500; extra cartridges cost $80 each. Not to be outdone, SunDisk has pared away excess PCMCIA packaging, producing a 1.4×1.7×0.13-in. flash-memory cartridge that users can plug into a PC Card adapter or directly into systems with the proper socket.



DataFab's $75 Mobile Disk adapter is only one of many kinds of adapters you can get to plug PC Cards into any computer.

However, these disks lack one essential feature. Disk makers report that, for the first time, they are getting repeat orders. Normally, customers buy a disk, install it in their PC, and never need another one. But PC Card hard disks are so small that people frequently lose them. Clearly, PC Card hard disks need a locator feature similar to the beepers that aid in finding remote controls and cordless phones.

PCMCIA HARD-DISK DRIVES

disks spin up, they avoid "stiction"—a nasty effect combining sticking and friction. High humidity and temperature aggravate stiction, causing disks to stop cold under worst-case conditions. Manufacturers of start/stop-contact disks intentionally roughen platter surfaces to avoid stiction.

Smooth and small

Intégral PC Card hard disks' platters have especially smooth, polished surfaces that enhance the micro-aerodynamics of the disks' flying heads. The polished surfaces permit the heads to fly 1.2 μin. above the platter on an air bearing vs the 3 μin. that 2.5- and 3.5-in. disks require. This low flying height permits the disk to put down smaller magnetic domains, allowing denser packing of data and increasing disk capacity.

PC Card hard disks also have to make room for disk-controller electronics that once filled an entire pc board. IC packaging varies widely from maker to maker. Intégral, for example, uses no standard packaging. The company's disks retract the head actuator completely off the platter, and the retracted actuator takes up room inside the PCMCIA package that start/stop-contact disks can use for electronics. The company uses modern, strenuous packaging technologies, such as multichip modules and chips on boards.

Maxtor, on the other hand, rolled over the electronics it developed for larger disks into its PC Card disks because it had already shrunk its electronics. The company uses a Texas Instruments' DSP μP as the heart of its disk controller. The controller has only five ICs: the DSP μP, an interface adapter, a TI dedicated-servo IC, a ROM, and a read/write-channel preamp IC. The company puts these five ICs onto a dual-sided, six-layer, 18-mil pc board mounted in the same plane as the platters. However, the DSP μP and the interface IC have custom pinouts that exactly match the PCMCIA connector, easing pc-board design and improving signal integrity. EDN

You can reach Senior Technical Editor Charles H Small at (617) 558-4556, as EDNSMALL on MCI Mail or the EDN Readers' BBS, and as ednsmall@mcimail.com on Internet.

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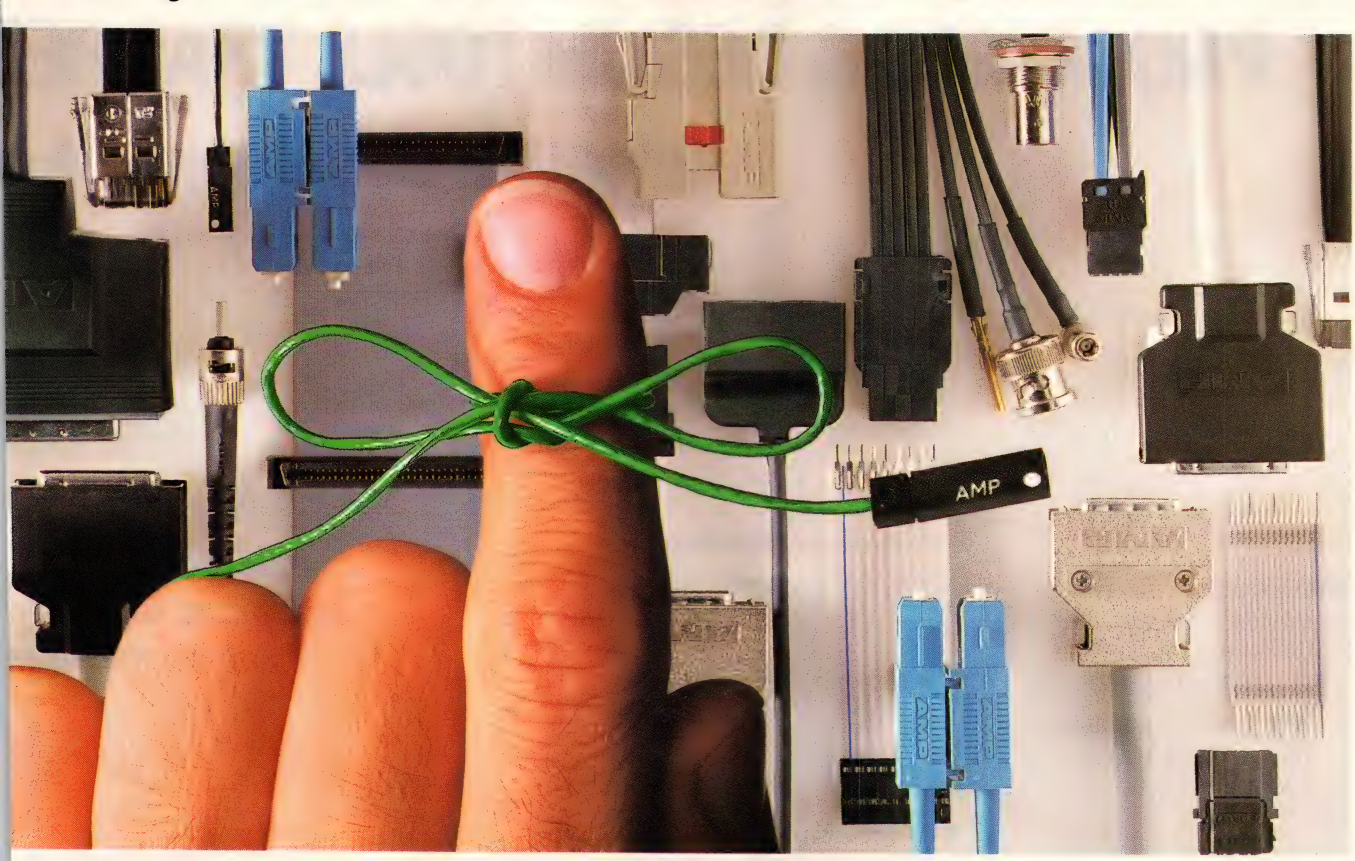
Circle No. 324

Lots of cable assemblies. Only one name to remember. AMP.



Cutting edge digital. Garden-variety ribbon. High-performance fiber. Whatever your cable assembly needs – from the standard to the technologically advanced – there's only one company to call. AMP.

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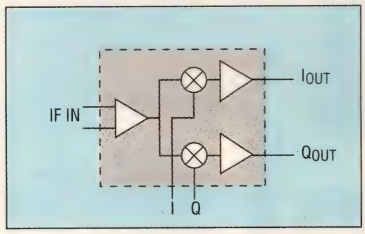
Precision Quadrature Demodulator

FEATURES:

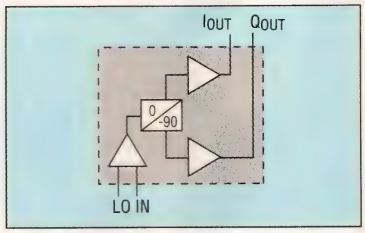
- Precise Quadrature Demodulation from 400MHz to 700MHz
- Wide Output Bandwidth
- Single 5V Supply



Quadrature Generator

FEATURES:

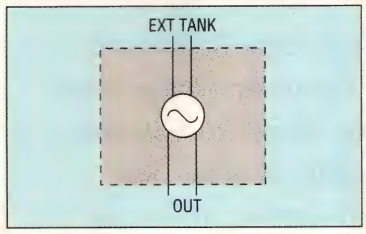
- Precision Quadrature Generation (< 1.5 deg, < 0.3dB at 650MHz)
- Wide Input Frequency Range (400MHz to 700MHz)



Differential Oscillator

FEATURES:

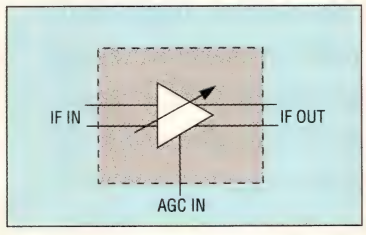
- Oscillates from < 400MHz to > 700MHz
- Low Phase Noise (-88dBc/Hz at 10kHz Offset, Qr > 20)
- Differential Resonator Port for Low Crosstalk



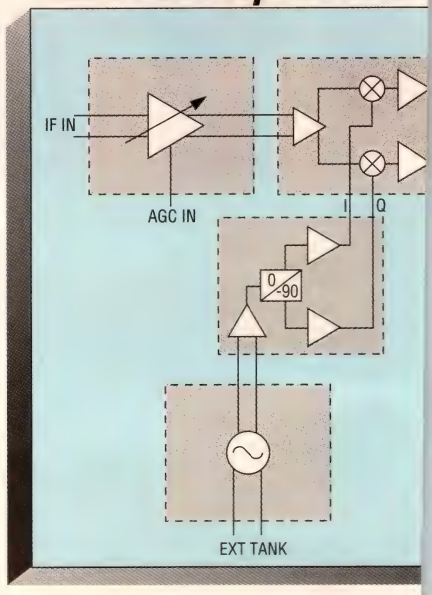
AGC Amplifier

FEATURES:

- Over 40dB of Gain Control Range
- Accepts IFs from 50MHz to 700MHz
- Single 5V Supply



MAX2101 6-Bit Quadrature Digitizer for TV Set-top Receiver



For More Information About the MAX2101, Call 1-800-998-8800

The MAX2101 subcircuits shown above form an excellent foundation for development of components that bridge the gap between existing RF downconverters and CMOS digital-signal processors. These subcircuits were developed using GST-1—Maxim's high-performance wafer fabrication process—and QuickTools—our powerful simulation and modeling software.

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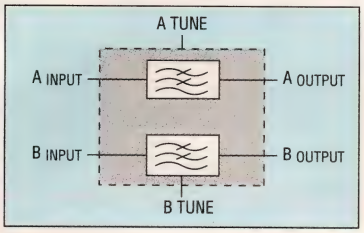
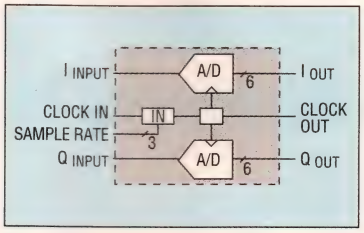


FEATURES:

- 5-Pole Butterworth Response
- Adjustable Cutoff Frequency
- Monolithic Construction for Inherent Match
- No External Components Required
- Single 5V Supply

Dual 6-Bit ADCs



FEATURES:

- Dual 6-Bit, 60Msps Flash Architecture
- Programmable Sample Rate
- Excellent Dynamic Performance (5.5 effective bits at f_{IN} = 15MHz)
- Monolithic Construction for Inherent Matching
- Single 5V Supply

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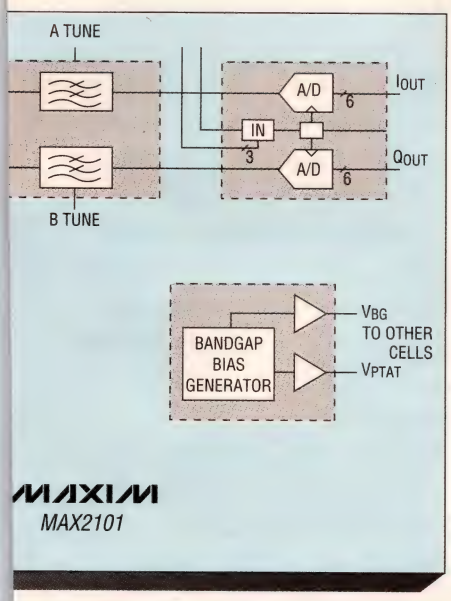
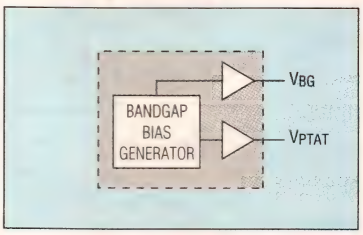


Bandgap Bias Generator



FEATURES:

- V_{BG}: ØT.C. (Temperature coefficient) Reference Voltage
- V_{PTAT}: P.T.A.T. (Proportional to Absolute Temperature) Reference Voltage
- Both Outputs Capable of Sourcing up to 1mA Load Current
- Single 5V Supply

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Used separately or in combination, the subcircuits can produce complete demodulation and digitization components for intermediate frequencies ranging from 400MHz to 700MHz and base bandwidths to 80MHz. Our GST-2 process with f_T to 27GHz is now available for custom design.

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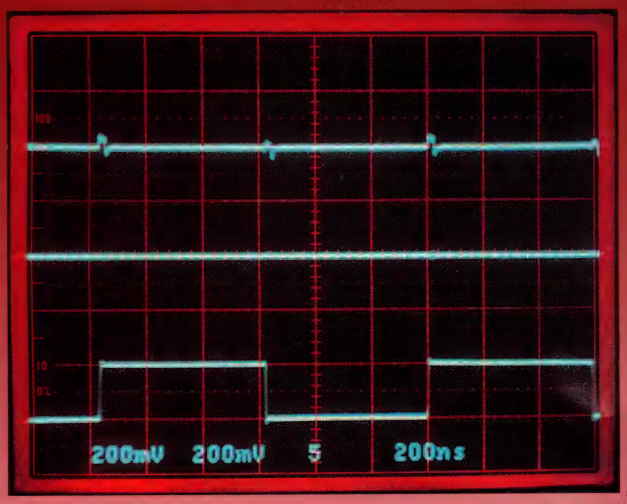
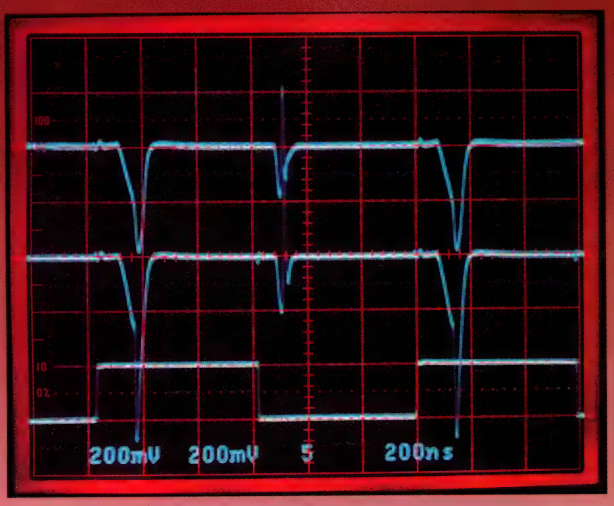
Switches Without Glitches.



Output

Input

Logic

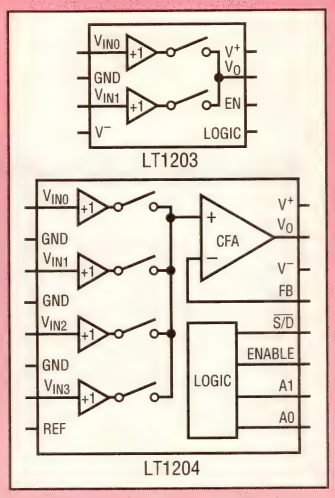


LT1203

CMOS MUX

LTC Video Multiplexers Have 90dB Isolation.

LTC's family of video multiplexers deliver professional quality solutions on your PC board without cascading switches to improve channel separation and isolation. The LT1203, LT1204 and LT1205 provide 90dB of isolation at 10MHz on real printed circuit boards. Forget those old switch buffers too, because all LTC multiplexers include buffers, are easily expandable and operate on ±5V to ±15V supplies. Switching glitches are almost invisible. The 2-input and 4-input LT1203/05 switch channels in only 25nsec and unlike CMOS switches, are virtually glitch-free at both output and input.



The LT1203/1205 are ideally suited for high speed graphics, multimedia, video routers or crosspoint applications delivering 150MHz bandwidth, 0.1dB gain flatness to 30MHz and Differential Gain/Phase of 0.02%/0.02° for true color fidelity.

For multiplexing where more output current is needed such as cable driving, the LT1204 4-input Video Multiplexer has an on-chip 75MHz Current Feedback Amplifier with 50mA output drive and 0.1dB gain flatness to 30MHz. A unique bootstrapping feature allows you to create larger multiplexers (8:1, 16:1) by just connecting the LT1204's outputs together, and you still get 90dB isolation at 10MHz on your PC board.

So, for multimedia, graphics or broadcast quality video, make LTC your first stop for ALL of your multiplexer needs. Pricing starts at $2.96 in 1000-piece quantities for the LT1203CS8. The LT1204CN is $4.78 and the surface mount LT1205CS starts at $5.06, both in 1000-piece quantities.

For details, contact Linear Technology Corporation, 1630 McCarthy Boulevard, Milpitas, California 95035/ 408-432-1900. For literature only, call **1-800-4-LINEAR.**

LINEAR TECHNOLOGY

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AND EVERYTHING IN BETWEEN.
CIRCLE NO. 105

EDITED BY CHARLES H SMALL & ANNE WATSON SWAGER

PSpice models nickel-metal-hydride cells

STEVEN C HAGEMAN, CALEX MANUFACTURING CO, CONCORD, CA

BBS

The nickel-metal-hydride (NiMH) battery model in **Listing 1** accurately predicts the discharge characteristics of an NiMH cell (or groups of cells). The model accounts for

- ampere-hour (Ahr) capacity of the cell
- cell resistance
- differing cell capacity, depending on low- and high-rate discharge characteristics.

The basic cell model is accurate for 0.001 to 5C discharge rates, where the 1C rate is a battery-industry term for the current that will discharge a cell to its cutoff voltage (usually 1.1V) in exactly one hour.

Fig 1's subcircuit is the basis for the cell model. You can probe four nodes of this subcircuit. *+OUTPUT* and *–OUTPUT* are the usual positive and negative terminals of the cell. You may connect these terminals to your circuit or connect the terminals in a series with other cells to model batteries.

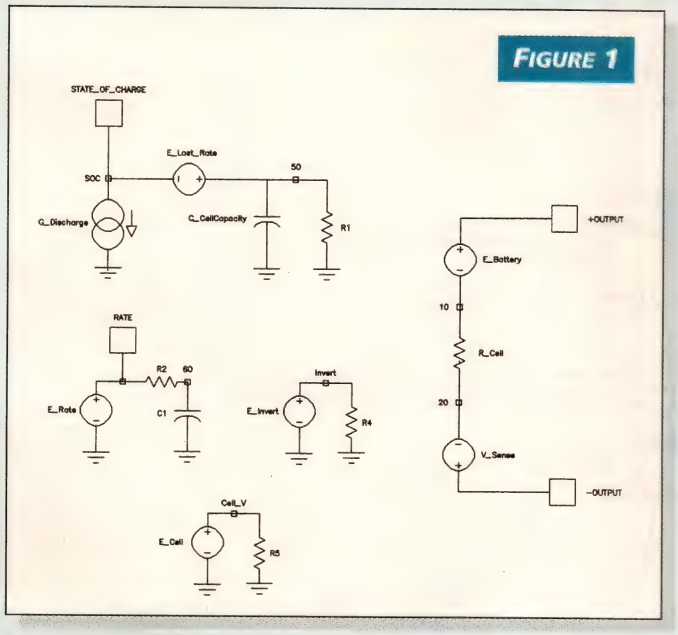
SOC is the state of charge of the battery at its present discharge rate. 1V at *SOC* indicates 100% state of charge; 0V represents no capacity remaining. Depending on the discharge rate, *E_LOST_RATE* lowers cell capacity at high rates of discharge. *RATE* is the instantaneous discharge rate of the cell in C units. So, 1V indicates that the battery is discharging at the 1C rate.

The parameters *CAPACITY* and *RESISTANCE*, passed to the NiMH subcircuit, represent the cell's nominal capacity and 100% charge. R2 and C1, connected to node 60, model a delaying action when *E_LOST_RATE* corrects the cell's capacity. You can see this effect in a real cell. A real cell initially exhibits a high terminal voltage that lasts for several seconds when first connected to a load. Then the cell's voltage quickly decays to a lower steady-state-discharge value.

LISTING 1—NiMH-CELL PSPICE MODEL

```
.SUBCKT NIMH
+ +OUTPUT -OUTPUT SOC RATE
;
;    |       |     |    |
;    |       |     |    +-- Instantaneous discharge rate, 1V=C, 10V=10C
;    |       |     +------ State of charge output node, 1V=100%, 0V=0%
;    +-------+------------ +/- Cell connections (Floating)
;
+  PARAMS: CAPACITY=1, RESISTANCE=1
;                |           |
;                |           +------------ Cell resistance in [uom]s
;                +------------ Cell capacity in ampere-hours,
;                              measured at 5-hour rate

E_Rate          RATE    0       VALUE = { I(V_Sense)/CAPACITY }
R2              RATE    60      1  ; R2-C2 provide 3 second delayed time
                                   ; constant
C1              60      0       3
E_LowRate       LowRate 0       TABLE { V(RATE) } = (0,0)
  (0.001,0.15)  (0.1,0.1) (0.2,0)
R3              LowRate 0       1G
G_LowRate       0       50      VALUE = { V(LowRate)*I(V_Sense) }
G_Discharge     SOC     0       VALUE = { I(V_Sense) } ; Discharge current
E_LostRate      50      SOC     TABLE { V(60) } = (0.2,0.0)
  (1.0,0.15)  (5,0.2)
C_CellCapacity  50      0       { 3600 * CAPACITY * 1.01 }
R1              50      0       1G
R_Cell          20      30      { RESISTANCE }
V_Sense         -OUTPUT 30      0
E_Invert        Invert  0       TABLE { V(SOC) } = (0,1) (1,0)
R4              Invert  0       1G
E_Cell          +OUTPUT 20      TABLE { V(Invert) } =
+(0.0000E+00  1.3346E+00) (7.0989E-03  1.3244E+00) (1.6327E-02  1.3144E+00)
+(2.9283E-02  1.3042E+00) (4.2593E-02  1.2942E+00) (6.8859E-02  1.2841E+00)
+(1.3008E-01  1.2733E+00) (4.3605E-01  1.2633E+00) (5.1165E-01  1.2532E+00)
+(5.8033E-01  1.2432E+00) (6.4635E-01  1.2331E+00) (7.0190E-01  1.2231E+00)
+(7.5834E-01  1.2130E+00) (8.0324E-01  1.2030E+00) (8.3075E-01  1.1929E+00)
+(8.5116E-01  1.1828E+00) (8.6820E-01  1.1727E+00) (8.8310E-01  1.1627E+00)
+(8.9641E-01  1.1527E+00) (9.0848E-01  1.1425E+00) (9.1860E-01  1.1324E+00)
+(9.2730E-01  1.1223E+00) (9.3475E-01  1.1122E+00) (9.4167E-01  1.1021E+00)
+(9.4841E-01  1.0919E+00) (9.5480E-01  1.0817E+00) (9.6013E-01  1.0716E+00)
+(9.6439E-01  1.0615E+00) (9.6776E-01  1.0515E+00) (9.7060E-01  1.0407E+00)
+(9.7291E-01  1.0299E+00) (9.7486E-01  1.0190E+00) (9.7663E-01  1.0080E+00)
+(9.7823E-01  9.9782E-01) (9.8001E-01  9.8706E-01) (9.8196E-01  9.7630E-01)
+(9.8391E-01  9.6612E-01) (9.8586E-01  9.5606E-01) (9.8799E-01  9.4542E-01)
+(9.9012E-01  9.3524E-01) (9.9225E-01  9.2518E-01) (9.9420E-01  9.1498E-01)
+(9.9580E-01  9.0400E-01) (9.9687E-01  8.9186E-01) (9.9740E-01  8.7990E-01)
+(9.9775E-01  8.6280E-01) (9.9793E-01  8.4818E-01) (9.9811E-01  8.2718E-01)
+(9.9828E-01  7.9518E-01) (9.9846E-01  7.4066E-01) (9.9864E-01  6.4712E-01)
+(9.9882E-01  5.1380E-01) (9.9899E-01  3.3476E-01) (1.0000E+00  0.0000E+00)
.ENDS
```



In this NiMH-cell PSpice model, you can probe the cell's output terminals as well as its discharge rate and state of charge.

To use the model, connect the cell's output terminals to your load, initialize node 50 to the cell's desired state of charge (1V=100% charge), and set node 60 to zero, initially.

The two most common NiMH cell types are the 4/5A and AA types. These cells have capacities of 1.5 and 1.1 Ahr (5-hour rate) and resistances of 0.02 and 0.03Ω, respectively. Consult manufacturers's data to model other cell sizes. Use the manufacturers's listed 5-hour discharge rate in Ahrs for the parameter *CAPACITY*.

Note: When simulating series-connected cells, connect the *SOC* and *RATE* of each subcircuit cell to different nodes in your circuit. Do not connect these nodes in common between cells. The ZIPfile attached to **EDN BBS /DI_SIG #1646** contains documentation, schematics, a test circuit and test results, and the **listing**. (DI #1646) EDN

To Vote For This Design, Circle No. 345

Reference

1. Hageman, Steven, "Simple PSpice models let you simulate common battery types," *EDN*, October 28, 1993, pg 117. (Available on the EDN BBS /freeware SIG as MS697.)

Printer port hosts precision analog I/O board

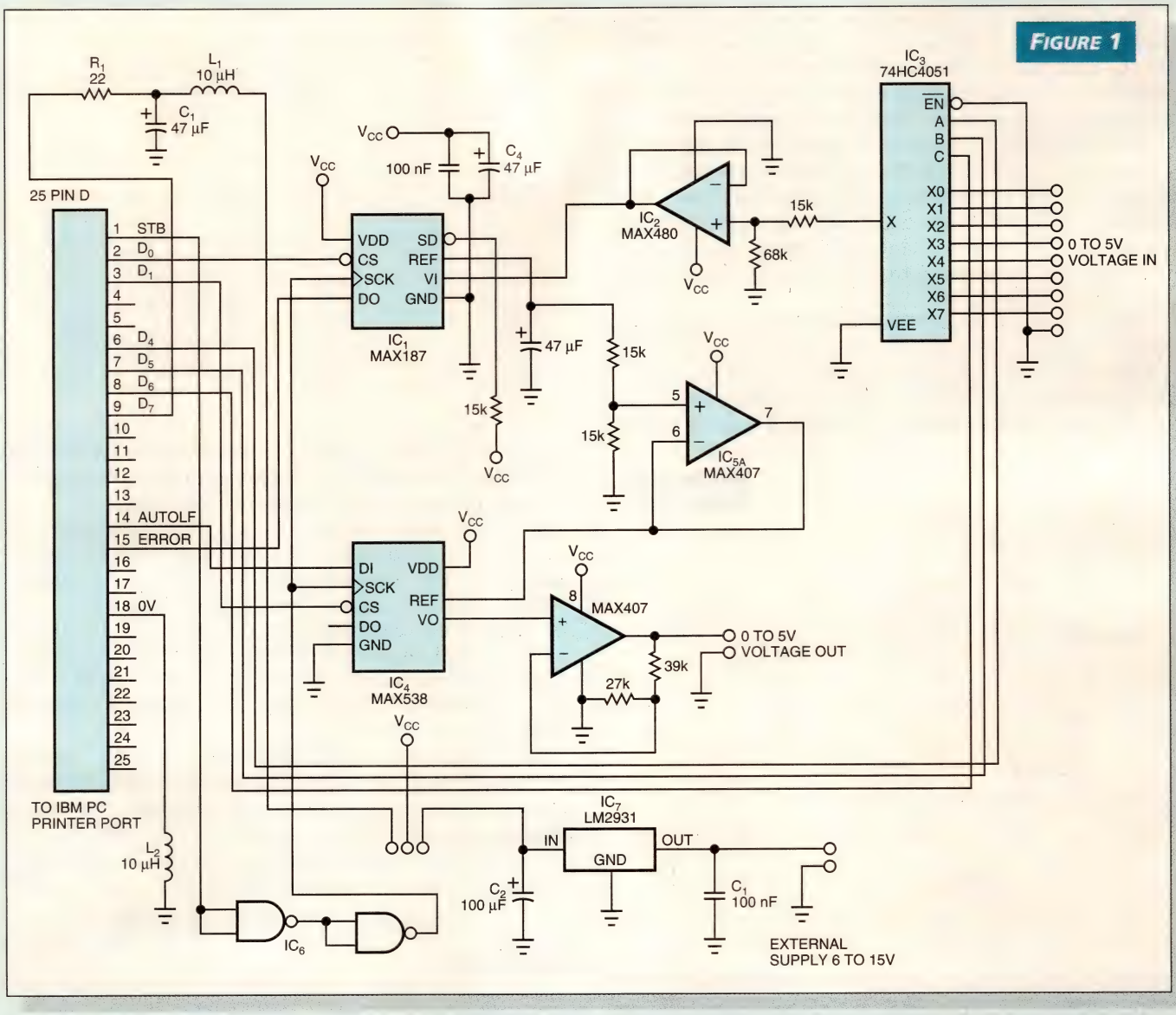
HUW JONES, GYRUS MEDICAL LTD, CARDIFF, WALES, UK

The 12-bit analog I/O board in **Fig 1** plugs into a PC's printer port. Thus, you can move the board around your laboratory more easily than you can exchange A/D boards that plug into the PC's backplane. The board handles eight 1-kHz input signals ranging from 0 to 5V max.

IC_1 is a serial, 12-bit A/D converter having an internal 4.096V reference and an internal track-and-hold circuit. Op-amp IC_2 provides a low-impedance source for IC_1. IC_2 has a V_{OS} of 70 µV, which is well within ½-bit conversion accuracy. Further, IC_2's rail-to-rail outputs come to within 1 bit of IC_1's full input range. However, the circuit's relatively slow slew rate limits input frequencies to below 1 kHz. Analog multiplexer IC_3 allows you to select any one of eight input channels.

D/A-converter IC_4 furnishes a 12-bit output. IC_4 derives its reference voltage from IC_1's reference output. Op-amp IC_{5A} and its associated components develop IC_4's 2.048V reference.

Schmitt-trigger IC_6 squares up the serial clock's edges (STB). This squaring up is a precaution and is, therefore,



This 12-bit analog I/O board plugs into a PC's printer port, allowing you to move the board around your laboratory easily.

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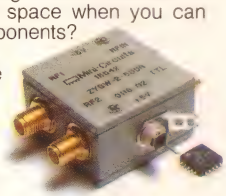
Truly incredible…superfast 3nsec GaAs SPDT reflective or absorptive switches with built-in driver, available in pc plug-in or SMA connector models, from only $14.95. So why bother designing and building a driver interface to further complicate your subsystem and take added space when you can specify Mini-Circuits' latest innovative integrated components?

Check the outstanding performance of these units…high isolation, excellent return loss (even in the "off" state for absorptive models) and 3-sigma guaranteed unit-to-unit repeatability for insertion loss. These rugged devices operate over a -55° to +100°C span. Plug-in models are housed in a tiny plastic case and are available in tape-and-reel format (1500 units max, 24mm). All models are available for immediate delivery with a one-year guarantee.



SPECIFICATIONS (typ)	Absorptive SPDT YSWA-2-50DR ZYSWA-2-50DR			Reflective SPDT YSW-2-50DR ZYSW-2-50DR		
Frequency (MHz)	dc-500	500-2000	2000-5000	dc-500	500-2000	2000-5000
Ins. Loss (dB)	1.1	1.4	1.9	0.9	1.3	1.4
Isolation (dB)	42	31	20	50	40	28
1dB Comp. (dBm)	18	20	22.5	20	20	24
RF Input (max dBm)	—	20	—	22	22	26
VSWR "on"	1.25	1.35	1.5	1.4	1.4	1.4
Video Bkthru (mV,p/p)	30	30	30	30	30	30
Sw. Spd. (nsec)	3	3	3	3	3	3
Price, $ (1-9 qty)	YSWA-2-50DR (pin) 23.95 ZYSWA-2-50DR (SMA) 69.95			YSW-2-50DR (pin) $14.95 ZYSW-2-50DR (SMA) 59.95		

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F141 REV. D

CIRCLE NO. 136

unnecessary if your PC has HCMOS-compatible output lines. Also, depending on your particular PC, printer-port-signal D_7 provides 5V power via R_1, C_1, and L_1. Obtain the best performance, however, by using an external supply. Low-dropout-regulator IC_7 yields a stable 5V from a 6 to 15V input. Inductor L_2 reduces digital noise from the PC's ground rail.

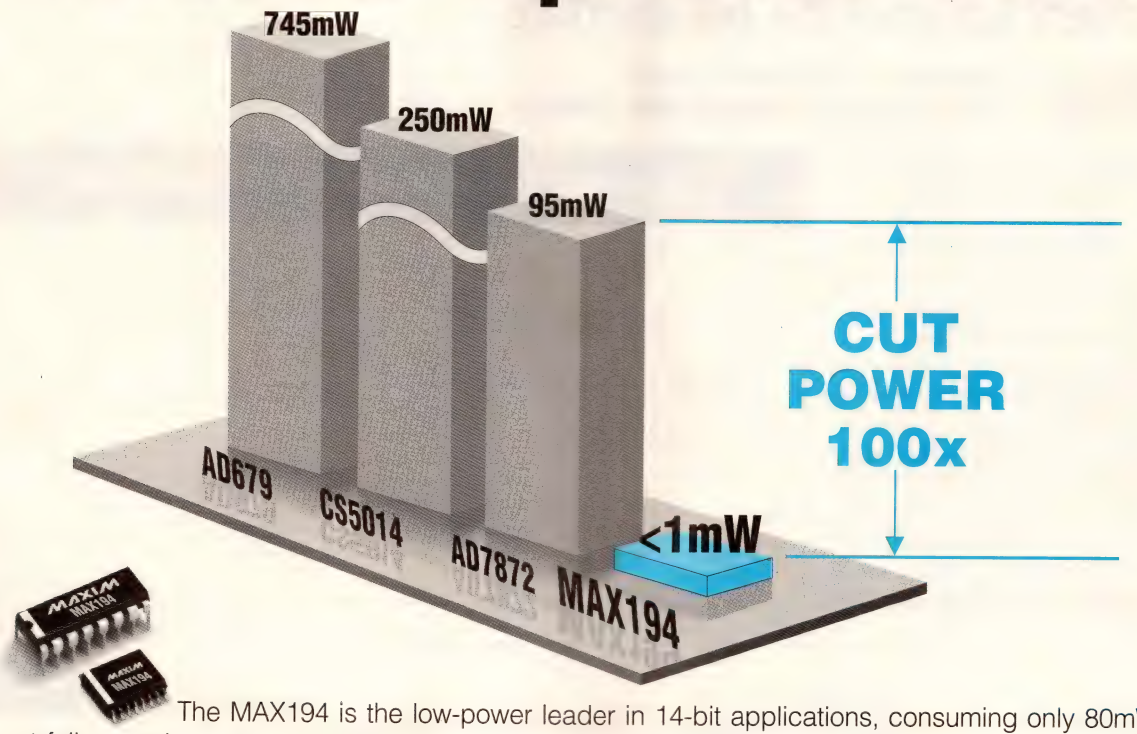
Listing 1 is a sample interface routine written in C++. You can easily convert this **listing** to standard C. A/D-conversion speed depends entirely on software-execution speed. The ZIPfile attached to **EDN BBS /DI_SIG #1647** contains the **listing** as well as a write-up. (DI #1647) EDN

To Vote For This Design, Circle No. 346

LISTING 1—SAMPLE CONVERSION C++ ROUTINE

```
#define STB 0x01        /* STROBE on pin 1 */
#define ALF 0x02        /* AUTO LINE FEED on pin 14 */
#define INIT 0x04       /* INITIALIZE on pin 16 */
#define SELO 0x08       /* SELECT OUT on pin 17 */
#define IRQ 0x10        /* INTERRUPT ENABLE bit */
#define BUSY 0x80       /* BUSY input on pin 11 */
#define ACK 0x40        /* ACK input on pin 10 - this is inverted */
#define PAPER 0x20      /* PAPER ok input on pin 12 */
#define SELI 0x10       /* SELECT IN pin 13 */
#define PERROR 0x08     /* ERROR signal on pin 15 */
#define D00             // data line declarations
#define D11
#define D22
#define D33
#define D44
#define D55
#define D66
#define D77
#define HIGH 1
#define LOW 0

enum onoff {high = 1, low = 0} ;   /* for bit control */

#include <dos.h>
#include <conio.h>
#include <iostream.h>

//*** read byte back from of selected printer data port ***
//* entry : printer port [1,2]
//* exit  : value read back from selected data port
char datain(int ppnum)
{
   int addr = 0x378 ;
   if (ppnum != 1)
       addr = 0x278 ;    // unless explicit port 1 , use port 2
   return(inportb(addr)) ;  // will be previously written data
}

//*** general purpose adjust control bit for selected printer port ***
//* entry : printer port [1,2], port bit as bitmask for control
//* exit  : control pin changed on selected port
void control_bit(int ppnum,char bitmask, onoff state)
{
   int addr = 0x378+2 ;
   char temp ;
   if (ppnum != 1)
      addr = 0x278+2 ;       // unless explicit port 1 , use port 2
   temp = inportb(addr) ;    // reads backs last control value from register
   temp ^= 0x0b ;            // bit inversion correction
   if (state == low)
      temp &= bitmask ;      // clear pin, no check for integrity
    else
      temp |= bitmask ;      // set pin high
   temp ^= 0x0b ;            // resurrect inversion
   outportb(addr,temp) ;     // written
}

//*** general purpose adjust data bit for selected printer port ***
//* entry : printer port [1,2], port bit number
//* exit  : data pin changed on selected port
   void data_bit(int ppnum, int bitnum, onoff state)
{
   int addr = 0x378 ;
   char temp ;
   char bitmask ;
   bitmask = (1 << bitnum) ;  // derive mask
   if (ppnum != 1)
              addr = 0x278 ;       // unless explicit port 1 , use port 2
   temp = inportb(addr) ;       // reads back register
   if (state == low)
      temp &= bitmask ;         // clear pin, no check for integrity
    else
      temp |= bitmask ;         // set pin high
   outportb(addr,temp) ;        // written
}

//*** read status byte of selected printer port ***
//* entry : printer port [1,2]
//* exit  : value obtained from selected status port
char statin(int ppnum)
{
   int addr = 0x378+1 ;
   if (ppnum != 1)
       addr = 0x278+1 ;              // unless explicit port 1 , use port 2
   return(inportb(addr)) ;   // status available in bits 7-3
}

//*** write data byte to bits D0-D7 of selected printer port ***
//* entry : printer port [1,2], data to be written
//* exit  : selected port written
void dataout(int ppnum,char data)
{
   int addr = 0x378 ;
   if (ppnum != 1)
       addr = 0x278 ;              // unless explicit port 1 , use port 2
   outportb(addr,data) ;      // written
}

//*** set up a/d input channel selection on D6-D4 ***
//* entry : port 1/2 and channel in range 0 to 7
//* exit  : HC4052 multiplexer routed
void mux(int port,int chan)
{
   char temp ;
   temp = datain(port) ;
   temp &= 0x8f ;                // mask out bits 4 through 6
   temp |= (chan << 4) ;
   dataout(port,temp) ;
}

//*** control synthesised Vcc rail powered from D7 ***
//* entry : port 1/2 and condition
//* exit  : power rail enabled/disabled with time lag
void power(int port, onoff state)
{
   if (state == high)
      data_bit(port D7,high) ;   // enable 5V
    else
      {
       control_bit(port,STB,low) ;  // set all control lines at 0V before
       control_bit(port,ALF,low) ;  // removing 5V supply
       mux(port,0)     ;            // same for data lines
       data_bit(port D0,low) ;
       data_bit(port D1,low) ;
       data_bit(port D7,low) ;      // now switch off 5V
      }
   delay(200) ;
}

//*** perform a serial clock pulse ***
//* entry : port 1/2, SCLK low
//* exit  : one clock pulse L->H->L generated
void clockbit(int port)
{
   control_bit(port,STB,high) ;   // force serial clock line high
   control_bit(port,STB,low) ;    // now low
}

//*** read 12 bit a/d input via MAX187 ***
//* entry : port 1/2, CS for a/d high,serial clock line low
//* exit  : 12 bit value in range 0-4095
int read_adc(int port)
{
   int clocks ;
   int adin = 0 ;
   int temp,timeout ;
   data_bit(port D0,low) ;      //chip select MAX187 via D0 going low
   timeout = 1000 ;
   do
   {
     temp = statin(port) & PERROR ;  // wait for busy to complete
     timeout-- ;
   }
   while ((!temp) && (timeout)) ;  // ready when DO goes low to high

   for (clocks = 0 ; clocks < 12 ; clocks++)   // read 12 bit data plus
     {                                         // one redundant
       adin <<= 1 ;             // adjust for msb bit shift out from MAX187
       clockbit(port) ;         // toggle serial clock
       if (statin(port) & PERROR)
         adin |= 0x01  ;        // shift in a 1 bit
     }
  clockbit(port) ;              // final redundant clock to complete
  data_bit(port D0,high) ; // disable MAX187
  return(adin) ;
}

//*** write 12 bit d/a via MAX538 ***
//* entry : port 1/2, voltage out value (0-4095) , CS for d/a high
//* exit  : d/a updated
void write_dac(int port,int dacval)
{
   int clocks ;
   int mask = 0x0800 ;
   control_bit(port,ALF,low) ;  //set data low
   data_bit(port D1,low) ;      // chip select MAX538 via D1 going low
   for (clocks = 0 ; clocks < 12 ; clocks++)   // write 12 bit data
     {                                         //set data on AUTO LINE FEED
      (dacval & mask) ? control_bit(port,ALF,high) : control_bit(port,ALF,low)
        ;
       clockbit(port) ;         // toggle serial clock
       mask >>= 1 ;     // realign mask for msb first operation
     }
   data_bit(port D1,high) ;   // disable MAX538
}

//*** test out main routine ***
main()
      {
   int port ;
   int i,temp ;
   int dac,adc ;
   port = 1 ;                   // assume LPT1:
   power(port,high) ;           // enable 5V rail
   mux(port,0) ;                // select a/d channel 0
   clrscr() ;
   dac = 0 ;
   while (! kbhit())            // loop until key press
   {
     write_dac(port,dac) ;  // 12 bit d/a saw tooth output
     dac++ ;
     if (dac > 4095)
       dac = 0 ;
     adc = read_adc(port) ;  // read 12 bit a/d
     gotoxy(10,5) ;
     cout << "a/d input = " << adc / 1000 << '.' << adc % 1000 << "V    " ;
   }
   power(port,low) ;            // disable 5V rail
}
```

LOWEST POWER, 85ksps 14-BIT ADC HAS 10µA SHUTDOWN



The MAX194 is the low-power leader in 14-bit applications, consuming only 80mW at full operating speed. And because it's the only device in its class with a shutdown mode, the MAX194 allows power consumption to drop even further at slower sampling rates. For example, the average power consumption at 1ksps is less than 1mW, as shown above.

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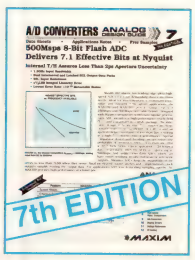

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CIRCLE NO. 108

PAL powers universal ISA bus interface

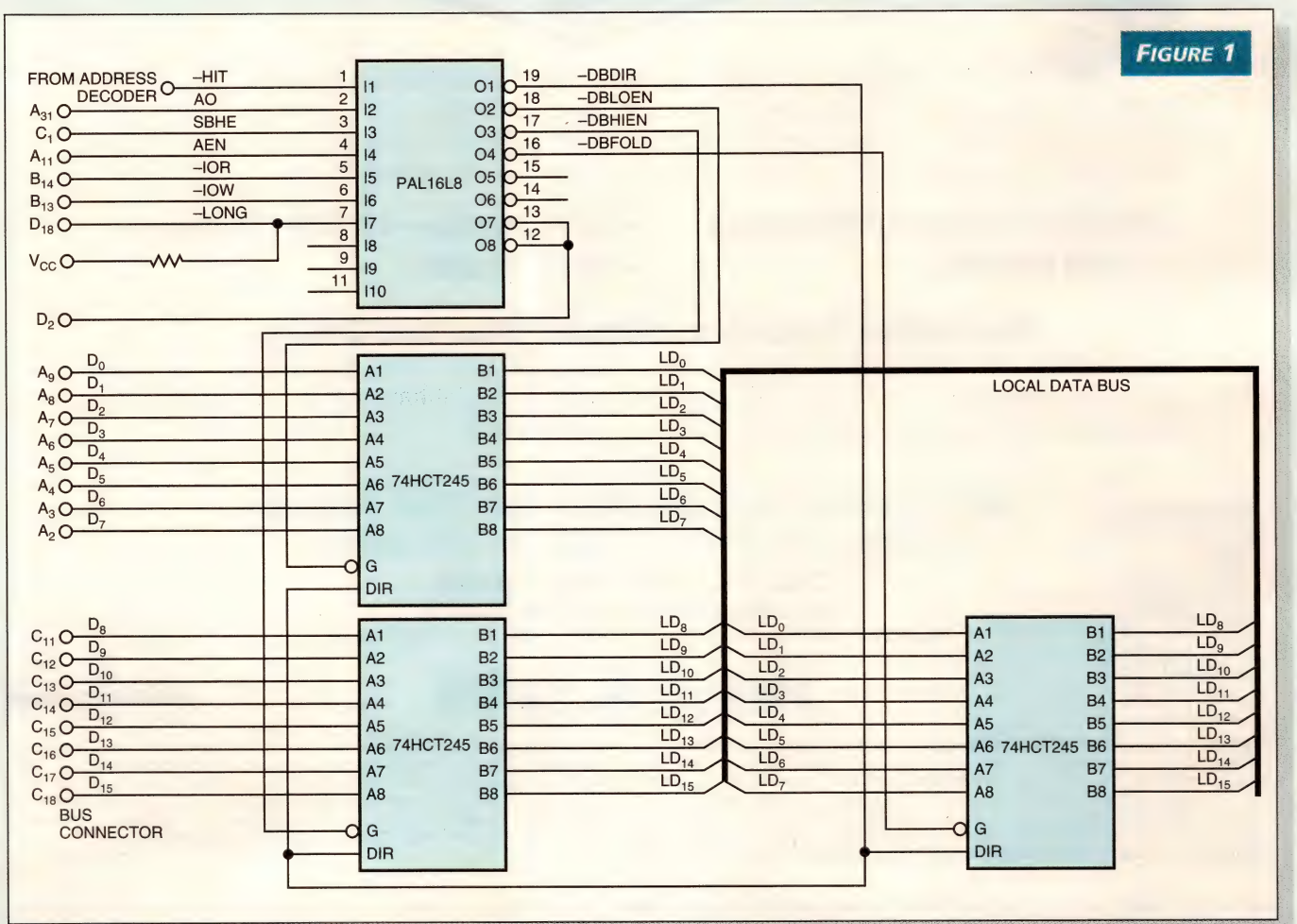
**JERZY R CHRZĄSZCZ, INSTITUTE OF COMPUTER SCIENCE,
WARSAW UNIVERSITY OF TECHNOLOGY, NOWOWIEJSKA, WARSAW, POLAND**

A pc board bearing the 16-bit ISA databus interface in **Fig 1** can adapt automatically to either 8- or 16-bit motherboard slots. The interface comprises three bidirectional octal buffers and glue logic. The glue logic controls transfer direction and output enables.

The logic integrated into the PAL16L8 distinguishes between 8- and 16-bit cycles using the state of the following signals: the LSB address bit (AO), the bus-high-enable flag (SBHE), the address-enable (AEN), and I/O-access strobes (–IOR and –IOW). A single resistor across V_{CC} and pin D_{18} of the ISA's secondary socket senses if the user has

LISTING 1—GLUE-LOGIC PAL PROGRAM

```
dbdir =>
    ior

dbfold =>
   a0 & !aen & hit & !ior & iow & !long
  # a0 & !aen & hit & ior & !iow & !long

dbhien =>
    !aen & hit & !ior & iow & long & !sbhe
  # !aen & hit & ior & !iow & long & !sbhe

dbloen =>
    !aen & hit & ior & !iow
  # !aen & hit & !ior & iow

iord16 =>
    1

iord16.oe  =>
    !a0 & !aen & hit & ior & !iow & long & !sbhe

iowr16 =>
    1

iowr16.oe  =>
    !a0 & !aen & hit & !ior & iow & long & !sbhe

read =>
    !aen & hit & ior & !iow

word =>
    !a0 & long & !sbhe

write =>
    !aen & hit & !ior & iow

dbdir.oe  =>
    1

dbfold.oe  =>
    1

dbhien.oe  =>
    1

dbloen.oe  =>
    1
```



This simple design forms the core of a universal ISA bus interface.

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CIRCLE NO. 109

plugged the board into an 8- or 16-bit slot.

The PAL generates the signal –IOCS16 to indicate the ability to make 16-bit transfers. If, during a 16-bit I/O access, the board does not assert –IOCS16, the motherboard's bus controller performs an additional byte cycle, allowing the high data byte to pass via bus lines D_0 through D_7.

This design is only the core of the interface (note the several unused PAL pins). But, starting with it, you can develop more sophisticated functions, assert wait states, support DMA cycles, and so on. If you migrate the design to 24-pin PLDs, you could even afford an on-chip, 10-bit I/O-address decoder. (DI #1648) EDN

To Vote For This Design, Circle No. 347

Program flags dangerous DOS commands

M N JAYARAM, BARC, BOMBAY, INDIA

BBS Windows users still perform many small housekeeping tasks, such as renaming, moving, or deleting files, by switching to DOS, because DOS is much faster than the time-consuming, icon-driven facilities of Windows.

However, you should not use certain DOS features, such as *CHKDSK* or tape backup, when Windows is running. Windows, because it is a multitasking operating system, maintains several open and swap files. Any changes to the FAT (file-allocation table) or directory structure may result in loss or corruption of data.

You can pre-empt the dangerous DOS commands by providing an appropriate *.COM* driver program to kick off the corresponding *.EXE* file. **Listing 1** shows a debug script, *safedos.scr*. To create the file *CHKDSK.COM*, for example, execute the DOS command:

debug <safedos.scr

Because files with *.COM* extensions receive higher priority than files with *.EXE* extensions, DOS will execute the program *CHKDSK.COM* when you enter *CHKDSK*. To create other *.COM* files to kick off their corresponding *.EXE* files, change the lines

db 'c:\dos\chkdsk.exe',0
nchkdsk.com

in debug-script *safedos.scr* appropriately.

An environment variable called *windir* exists when Windows is running. This environment variable is unique because it is the only environment variable stored in lower case. All other environment variables are in upper-case characters. (DOS's *SET* command can create environment variables in upper case only.) The program scans the "environment" (DOS-ese for a reserved section of memory) for the environment-variable *windir*. If found, the program exits with the error message "Shutdown Windows!". Otherwise, the program loads and executes c:\dos\chkdsk.exe.

Because a *.COM* program assumes that it is the sole owner of the entire memory, you must free the memory not needed by the program so that it can safely and successfully execute a child process. Before freeing the additional memory, you must move the stack pointer to within the program area. The text attached to **EDN BBS /DI_SIG #1650** contains the program and documentation. (DI #1650) EDN

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LISTING 1—DEBUG-SCRIPT SAFEDOS.SCR

```
a100
mov bx,40
mov sp,3fe
mov wo[3fe],0
mov ah,4a
int 21
mov ax,[2c]
dec ax
mov ds,ax
mov ax,[3]
push cs
pop ds
mov cl,4
shl ax,cl
mov cx,ax
mov bx,2c
mov es,[bx]
mov al,[017b]
xor di,di
repne
scasb
jcxz 0141
es:
mov al,[di]
cmp al,[017c]
jnz 0141
lea dx,[017d]
mov ah,9
int 21
ret
lea dx,[01b2]
push cs
pop es
mov ax,cs
mov [01a8],ax
mov ax,0080
mov [01a6],ax
lea bx,[01a4]
mov [01a0],ss
mov [01a2],sp
mov ax,4b00
int 21
jnc 016d
mov ah,9
lea dx,[0191]
int 21
mov ax,[01a0]
mov bx,[01a2]
cli
mov ss,ax
mov sp,bx
sti
ret
db 'r='
db 7,'Shutdown Windows! $'
db 'Exec failed ! $'
dw 0
dw 0
dw 0
dw 0
dw 0
dw ffff
dw ffff
dw ffff
dw ffff
db 'c:\dos\chkdsk.exe',0

nchkdsk.com
rcx
100
w
```

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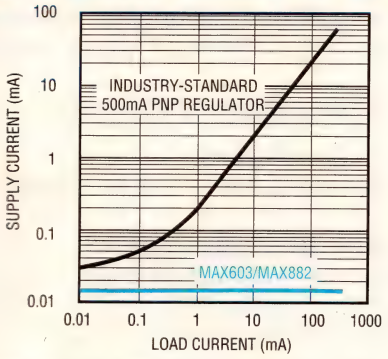
The MAX603/MAX882 family of linear regulators uses P-channel MOSFET transistors and high-power packaging to reduce size, increase battery life, and extend operating range. Maxim's P-channel design keeps supply current low, even at high output current and at low input-to-output differentials where the PNPs in bipolar low-dropout regulators saturate.

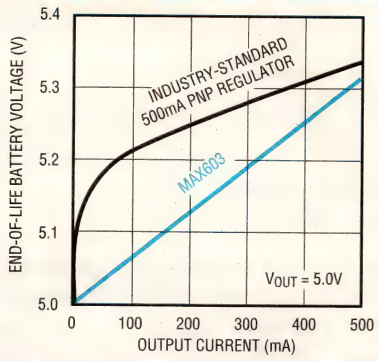
- **1.8W High-Power 8-Pin SO Package**
- **15µA Supply Current at I_{OUT} = 500mA**
- **2µA Shutdown Current**
- **2.7V to 11.5V Input Voltage Range**
- **1.3V to V_{IN} Output Voltage Range**
- **Low Dropout Voltage (320mV at 500mA)**
- **Thermal Shutdown, Reverse Current & Short-Circuit Protection**
- **500mA (MAX603/MAX604)**
  200mA (MAX882/MAX883/MAX884)

LOWEST SUPPLY CURRENT AT ALL LOADS



Maxim's P-channel design draws only 15µA, unlike bipolar low-dropout regulators, which consume up to 60mA at full load and waste up to 0.5W of additional power.

LOWEST DROPOUT VOLTAGE



Low dropout voltage extends useful battery life.

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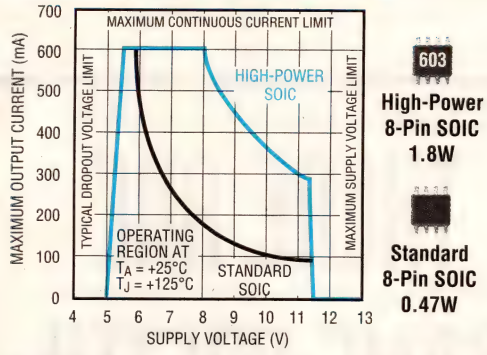
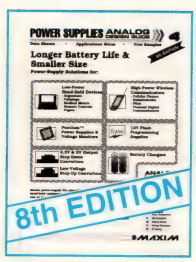


Special packaging extends the output current and input voltage range and lets these regulators fit in a standard 8-Pin SOIC (<0.05 in²).



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CIRCLE NO. 110

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The winning Design Idea for the August 18, 1994, issue is entitled "$10 receiver has microvolt sensitivity," submitted by Charles Kitchin of Analog Devices (Wilmington, MA).

LINEAR TECHNOLOGY

DESIGN NOTES

LTC1451/52/53: 12-Bit Rail-to-Rail Micropower DACs in an SO-8

Design Note 96

Hassan Malik and Jim Brubaker

The LTC®1451, LTC1452 and LTC1453 are complete, single supply, rail-to-rail voltage output 12-bit digital-to-analog (DAC) converters. They include an output buffer amplifier and a space saving SPI compatible three-wire serial interface. There is also a data output pin that allows daisy-chaining multiple DACs. These DACs use a proprietary architecture which guarantees a DNL (Differential Nonlinearity) error of less than 0.5LSB. The typical DNL error is about 0.2LSB as shown in Figure 1. There is a built-in power-on reset that resets the output to zero scale. The output amplifier can swing to within 5mV of V_{CC} when unloaded and can source or sink 5mA even at a 4.5V supply. These DACs come in an 8-pin PDIP and SO-8 package.

5V and 3V Operation

The LTC1451 has an on-board reference of 2.048V and a nominal output swing of 4.095V. It operates from a single 4.5V to 5.5V supply dissipating 2mW ($I_{CC(TYP)}$ = 400µA).

The LTC1452 is a multiplying DAC with no on-board reference and a full-scale output of twice the reference input. It operates from a single supply that can range from 2.7V to 5.5V. It dissipates 1.125mW ($I_{CC(TYP)}$ = 225µA) at a 5V supply and a mere 0.5mW ($I_{CC(TYP)}$ = 160µA) at a 3V supply.

The LTC1453 has a 1.22V on-board reference and a convenient full scale of 2.5V. It can operate on a single supply with a wide range of 2.7V to 5.5V as shown in Figure 2. It dissipates 0.75mW ($I_{CC(TYP)}$ = 220µA) at a 3V supply. The digital inputs can swing above V_{CC} for easy interfacing with 5V logic.

True Rail-to-Rail Output

The output rail-to-rail amplifier can source or sink 5mA over the entire operating temperature range while pulling to within 300mV of the positive supply voltage or ground. The output swings to within a few millivolts of either

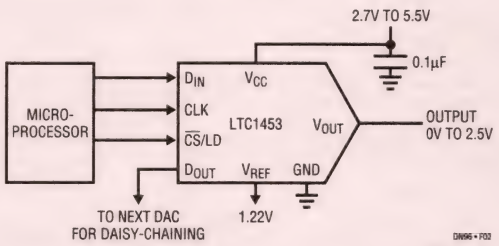
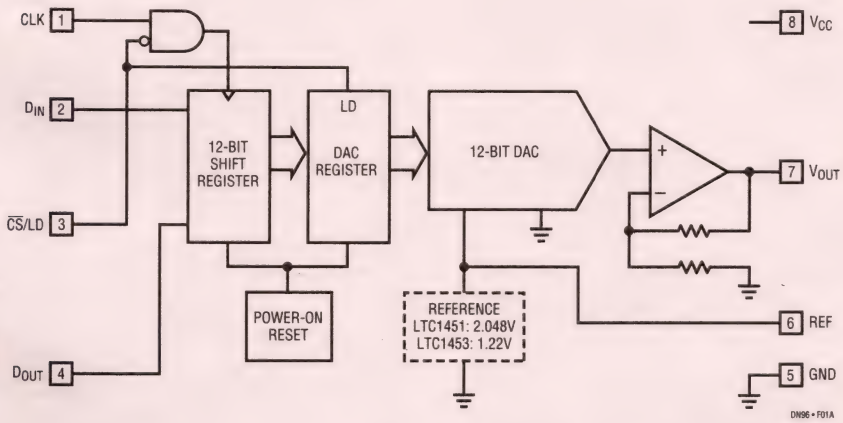


Figure 2. The 3V LTC1453 is SPI Compatible and Talks to Both 5V and 3V Processors



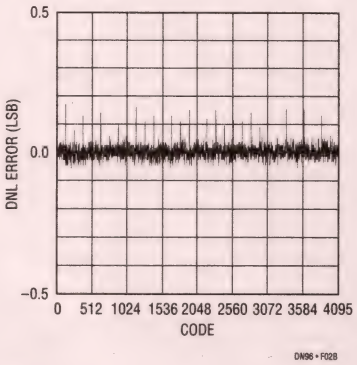


Figure 1. Proprietary Architecture Guarantees Excellent DNL

supply rail when unloaded and has an equivalent output resistance of 50Ω when driving to either rail. The output can drive a capacitive load of up to 1000pF without oscillating.

Wide Range of Applications

Some of the applications for this family include digital calibration, industrial process control, automatic test equipment, cellular telephones and portable battery-powered applications where low supply current is essential. Figure 3 shows how to use an LTC1453 to make an opto-isolated digitally controlled 4mA to 20mA process controller. The controller circuitry, including the opto-isolator, is powered by the loop voltage that can have a wide range of 3.3V to 30V. The 1.22V reference output of the LTC1453 is used for the 4mA offset current and V_{OUT} is used for the digitally controlled 0mA to 16mA current. R_S is a sense resistor and the LT®1077 op amp modulates the transistor Q1 to provide the 4mA to 20mA current through this resistor. The potentiometers allow for offset and full-scale adjustment. The control circuitry consumes well under the 4mA budget at zero scale.

Flexibility, True Rail-to-Rail Performance and Micropower; All In a Tiny SO-8

The LTC1451, LTC1452 and LTC1453 are the most flexible micropower, stand alone DACs that offer true rail-to-rail performance. This flexibility along with the tiny SO-8 package allows these parts to be used in a wide range of applications where size, power, DNL and single supply operation are important.

Table 1. LTC Serial Voltage Output DACs

Part	V_{CC} Range	Reference	Full Scale	I_{CC}
LTC1451	4.5V to 5.5V	2.048V-Internal	4.095V	400µA at 5V
LTC1452	2.7V to 5.5V	External	2 × REF	225µA at 5V
LTC1453	2.7V to 5.5V	1.22V-Internal	2.5V	250µA at 3V
LTC1257	4.75V to 15.75V	2.048V-Internal (2.5V to 12V-External)	2.048V (2.5V to 12V)	350µA at 5V

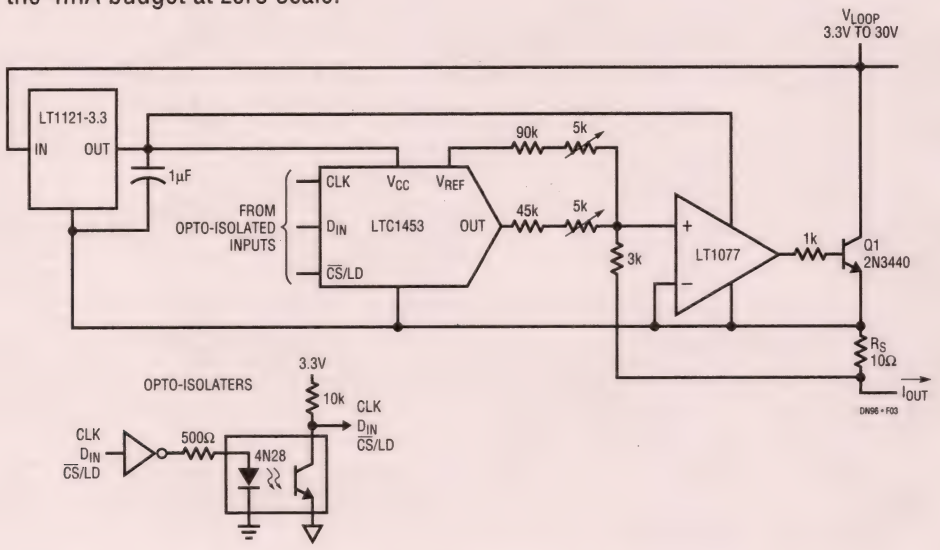


Figure 3. 4mA to 20mA Process Controller Has 3.3V Minimum Loop Voltage

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CIRCLE NO. 145

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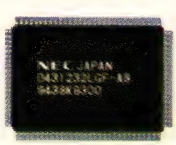

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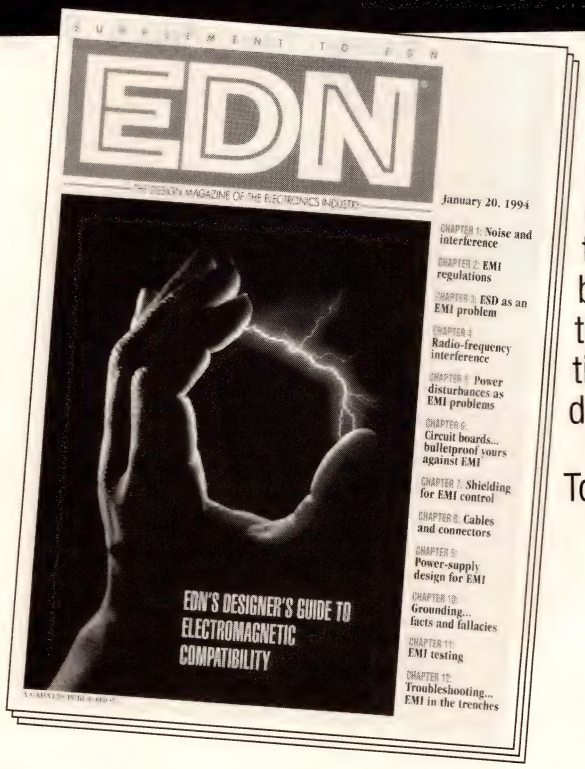

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Design considerations bring unity to a mixed-voltage world

KENNETH M CUY, ADVANCED MICRO DEVICES

If you design with low-voltage devices, you've probably encountered the compatibility issue of making systems operate with some 5V devices. A few design considerations, such as how to mix voltages, might bring your system into harmony.

The market for low-voltage (3.3V and below) systems is growing. One factor fueling this growth is the emphasis on protecting the environment: To save energy, "green" machines operate at lower voltages than do traditional devices. Technology is another driving force in the market. As IC technology advances, transistor geometries are decreasing to submicron sizes that cannot handle standard 5V voltages.

However, not every IC manufacturer has entered the still-emerging market for low-voltage devices. Until all manufacturers make the switch to low voltages, designers must take precautions to ensure proper operation of mixed 3/5V hybrids.

Currently, 3V devices dominate the markets for mobile computing and communications. This market comprises portable PCs, including notebook and subnotebook computers, and personal information devices, including handheld computers and electronic books. Mobile-communication products include cellular phones, pagers, and other personal communicators. Although the major thrust of 3V devices is for portable systems, desktop systems can still reap the advantages of lower voltages.

To succeed in the market for portable computing and communications, systems must offer low size and weight; energy efficiency for extended operating life; performance rivaling full-power systems but maintaining low-power systems' cost-effectiveness; user-friendly interfaces, such as voice, pen, and touch inputs; wireless-communications capability; ruggedness; and dependability.

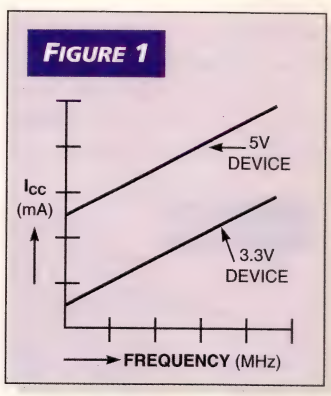
Power in hybrid designs is directly proportional to the square of the supply voltage. Thus, switching from a 5 to a 3V supply yields a 44% reduction in power, as the following equations show:

$$P_{3.3}=V^2/R=(3.3)^2/R=10.89/R$$
$$P_5=V^2/R=(5)^2/R=25/R$$
$$P_{3.3}/P_5=0.44=44\%,$$

where P=power, V=supply voltage, and R=resistance.

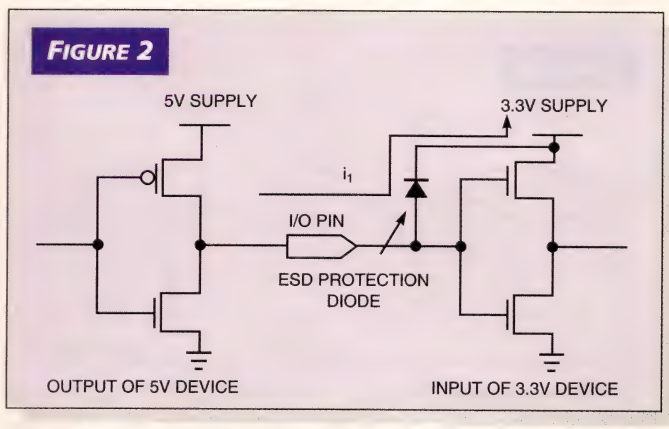
Because power, voltage, and current affect each other, the current decreases as the voltage decreases (**Fig 1**). For example, a 5V version of a 33-MHz Intel 486DX μP operating offers a 900-mA current rating, and a 3V version of a 33-MHz

FIGURE 1



Because power, voltage, and current affect each other, the current decreases as the voltage decreases, which contributes to a 44% power savings.

FIGURE 2



A 5V CMOS device driving a 3.3V CMOS device might forward-bias the ESD protection diode and cause excessive current.

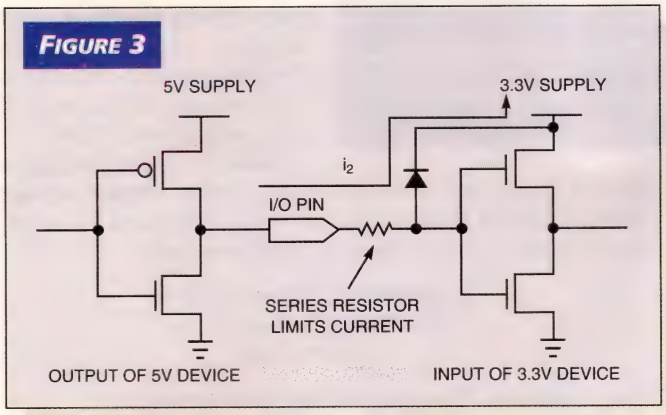
MIXED-VOLTAGE DEVICES

Advanced Micro Devices 486DX μP offers a 425-mA current rating. Switching to a 3V design causes the current requirements to drop by more than half. Because there are no major developments in battery technology, designers must build systems that run longer on existing power supplies. The lower voltage technology will help designers achieve that goal.

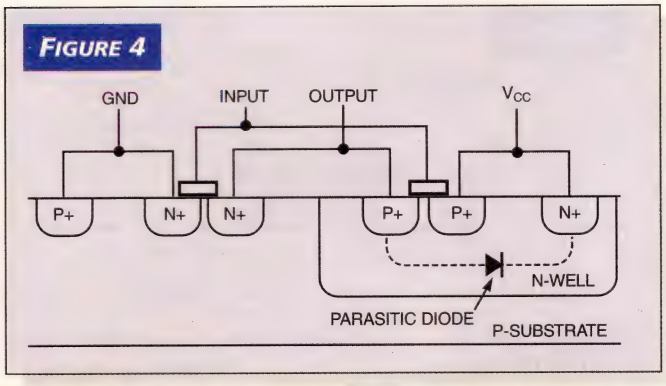
Lower voltages yield many benefits

Because the systems requires only 3.3V, unregulated power supplies, such as standard alkaline batteries, are sufficient to operate a system. Because systems no longer require large regulated power supplies, system form factors and weights also decrease, which is important in handheld and portable systems.

Switching to a 3V supply also reduces the output-voltage swings, making the systems produce less noise. The lower voltages also reduce EMI emissions and make them easier to control; as a result, standard-setting institutions, such as the FCC, will be more likely to approve 3V systems. In addition, 3V systems inevitably run cooler than 5V systems, leading to increased system reliability.



If board space is critical but speed is not, place a series resistor between the 3 an 5V devices to limit the current flowing from the 5V device into the 3V device.



Internally alter the the source and drain region of a true CMOS device to eliminate the parasitic diode, thus eliminating excessive current draw.

Pay careful attention to device placement and usage in a hybrid design. The following guidelines apply to a design that integrates 3.3 and 5V devices. Interfacing 3V TTL devices to 5V TTL devices typically causes no problem because the 3V TTL-device outputs have the same characteristics as those of the 5V TTL-device outputs.

Interfacing 3V TTL or CMOS devices to 5V CMOS devices, however, causes problems because the 5V devices need extra drive to prevent leakage current. Many voltage translation devices, such as Performance Semiconductor's PCT3 voltage-translation series, translate from 3.3 to 5V. However, this solution adds delay and board space.

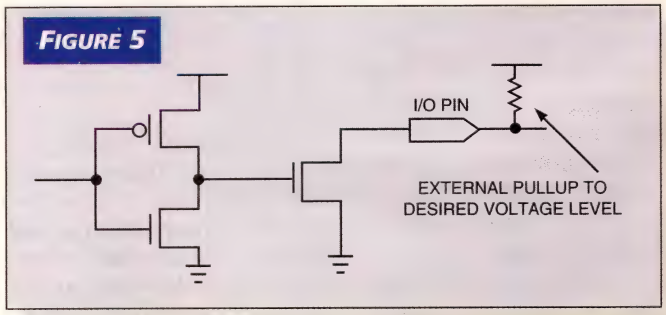
Interfacing 3V CMOS devices to 5V TTL devices doesn't compromise performance because the 3V device outputs have sufficient margin to drive 5V TTL-device inputs. However, you cannot directly connect a 5V output to a 3V input. Driving a 3V input, a 5V output can exceed the maximum supply-voltage rating and can forward-bias the ESD protection diode. The diode allows excess current to flow from the 5V device into the 3V power supply, possibly inducing latch-up (**Fig 2**). In this case, use voltage-translation devices.

Space-vs-speed trade-offs

If board space is critical but speed is not, you can place a series resistor between the 3 and 5V devices to limit the current flowing from the 5V device into the 3V device (**Fig 3**). The series resistor makes **Fig 3**'s i_2 less than **Fig 2's** i_1. However, if speed is critical, you should consider another method because adding a series resistor increases the device's propagation delay. Further, adding components increases board space and reduces noise immunity and system reliability.

Plan carefully when designing a system that requires devices of different voltages to reside on the same bus. In the previous scenarios, voltage translations were unidirectional, but a bus application requires bidirectional interfaces. One such interface, the Integrated Device Technology 74FCT164245, provides bidirectional 3-to-5V translation, with 3 or 5V signals driving the control inputs. Regardless of whether a 3V device resides on a 5V bus or a 5V device resides on a 3V bus, run the bus at one voltage and use translation circuitry and buffers between the other devices.

You can modify the input and output structures of a device so that internal voltage translations can occur. Occasionally, you can use a true CMOS transmission gate at the



Place an external pull-up resistor in the open-drain output of a CMOS device to accomplish the voltage translation.

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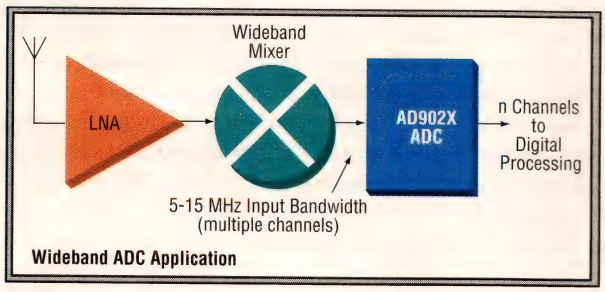

Wideband ADC Application

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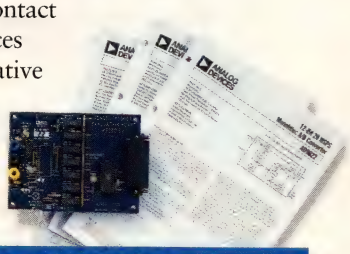

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CIRCLE NO. 17

MIXED-VOLTAGE DEVICES

output. A parasitic diode exists between the source/drain region and the diffusion well (**Fig 4**). If a 5V signal drives the I/O pin, the parasitic diode forward-biases and produces a path for current. By modifying the output structure to omit the pnp transistor, the input can now rise above 3.3V. Adding a transistor to an output structure prevents output latch-up, solving the problems that external translation circuitry cause.

Derating a 5V device for use as a 3V device may cause insufficient drive capability. The 3V devices operate at lower supply voltages, lowering the devices' output-drive capabilities. If you want to use these devices in bus applications, determine whether the parts are derated or truly low-voltage devices: A derated part often offers lower performance than that of an equivalent 5V device, whereas a true low-voltage design performs as well as or better than its 5V counterpart.

Another possibility for interfacing 5 and 3V devices is to use a device, such as Advanced Micro Devices' PALCE16V8HD, with an open-drain-output configuration. These devices act as buffers and ensure safe operation of 3.3V devices. However, a device with an open-drain option may have an internal pull-up transistor whose parasitic diode may forward-bias, causing current to flow. A true open-drain device requires only an external pull-up resistor to the desired voltage level (**Fig 5**).

Hybrid systems include multiple voltage supplies, so you must prevent latch-up on the I/Os during power-up and -down. To prevent latch-up on power-up, make sure that the 5V supply is greater than or equal to the 3V supply. To prevent latch-up on power-down, the 3V supply should be less than or equal to the 5V supply. Many chip sets, such as Pico Power's Evergreen HV PT86C268, run on dual power supplies and provide control signals for peripheral and system power planes. To take full advantage of the two voltage devices, mix the design on the board so that the speed-critical paths run at 5V and the low-power paths run at 3.3V.

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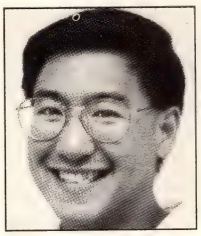
Author's biography



Kenneth M Cuy is an applications engineer at Advanced Micro Devices' Programmable Logic Division in Sunnyvale, CA, where he has worked for three years. In his current position, he provides applications support for Mach 3 and 4 devices. He has also helped develop CMOS PLDs, such as the 16V8, 20V8, and 22V10, and high-density Mach 1, 2, 3, and 4 devices. Cuy has a BSEE from Rensselaer Polytechnic Institute (Troy, NY), and lists photography and mountain biking as his hobbies.

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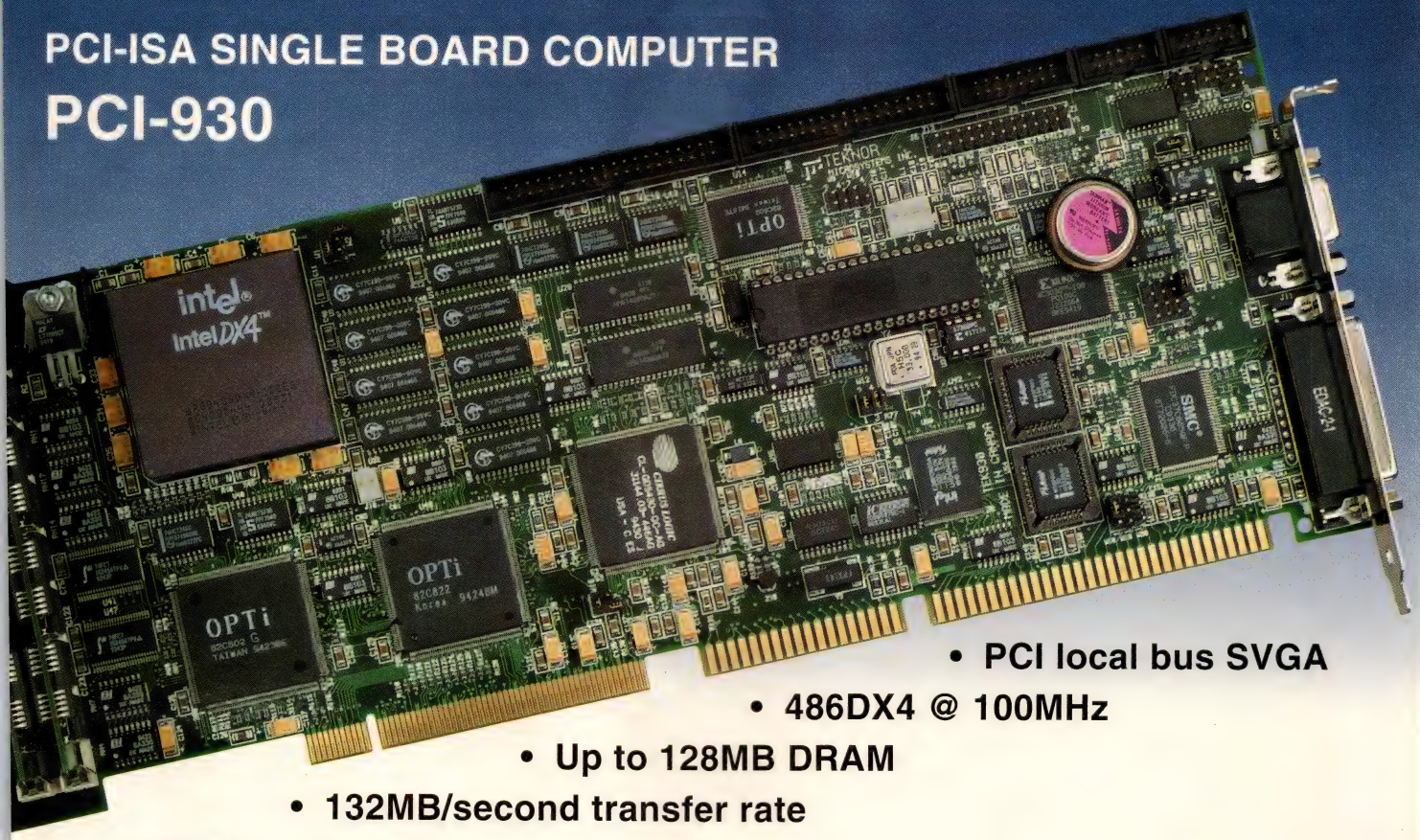

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CIRCLE NO. 36

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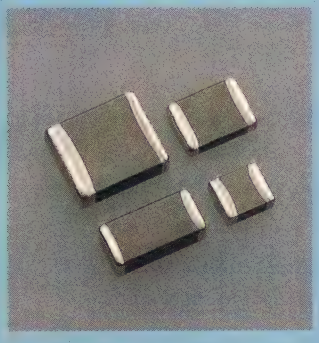
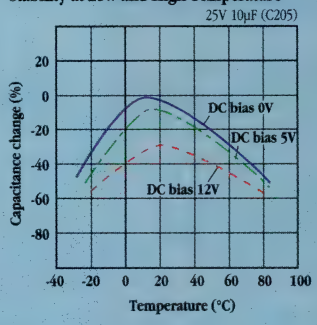


Capacitance Range [μF]

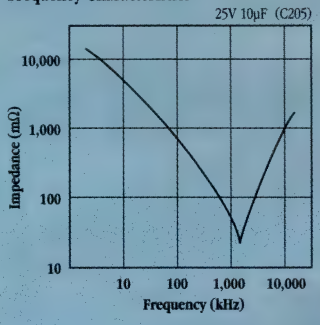
CAP (μF)	Rated Voltage (DC)					
	25V (IE)		50V (IH)		100V (2A)	
1	C103*	C203*	C203		C205	
1.5	*	*			C505	
2.2		*	C304	C205		
3.3	C205*	*				
4.7	*	C304*	C505			
6.8	*	*				
10	*	*				
15	C505					
18						
22						

End terminations Fired-on end termination : All case code
Metal plate end termination (nickel and solder) : *

Stability at Low and High Temperature



Frequency Characteristics



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CIRCLE NO. 147

Try *fixing it* yourself

JIM WILLIAMS, LINEAR TECHNOLOGY CORP

Drag out some of that obsolete electronic equipment collecting dust in storage. Your next cutting-edge innovation may come from tinkering with a relic of the past.

Fall of 1968 found me at the Massachusetts Institute of Technology (MIT), preparing courses, negotiating students' theses topics, and assembling a laboratory. My activities were fairly unremarkable behavior for the locale, but, for a 20-year-old college dropout, the circumstances were charged: This was my one shot at any sort of career. For reasons I'll never understand, my entire education, from kindergarten through college, had been a nightmare, perhaps the greatest impedance mismatch in history. When I got hot, the Detroit Board of Education didn't. Leaving Wayne State University after a dismal year and a half seemed to close the casket on my circuit-design dreams.

All this history conspired to provide me with an unusual outlook, a mix of terror and excitement. But mostly terror. Here I was, back in school, but on the other side of the lectern. Worse yet, my research project, although of my own choosing, seemed open-ended and unattainable. I was scared to death. The capper of this scenario was my social situation: I was younger than some of my students, and my colleagues had at least 10 years over me.

The architect of my unique opportunity was Jerrold R Zacharias, eminent physicist, Manhattan Project and Radiation Lab alumnus, and father of atomic time. Zacharias had waved the magic wand to get me an MIT appointment, a lab, and operating money. He also made it clear that he expected results. He was not the sort to tolerate looking foolish, and, in my mind, to fail him promised a far worse fate than dropping out of school.

Against this backdrop, I received my laboratory-budget request back from review. Zacharias permitted me untrammeled freedom. Everything I requested, even very costly items, had been approved without comment or question. He included just one restriction: no allocation

Daniel Guidera

FIX IT YOURSELF!

for instrument repair and calibration. His handwritten comment read, "You fix everything."

It didn't make sense. Under pressure for results, scared to pieces, I was supposed to waste time by screwing around fixing lab equipment? I went to see Zacharias. I negotiated. I pleaded. I ranted. But I lost. The last thing I heard chasing me out of his office was, "You fix everything."

I soon cooled off, and the issue became irrelevant because nothing broke. At least for a while. Finally, a high-sensitivity, differential-scope plug-in, a Tektronix 1A7, died. Life would never be the same.

Stealing isn't always a sin

The problem wasn't particularly difficult to find, once I took the time to understand how the thing worked. The manual's level of detail and writing tone were notable; communication was the priority. This seemed a significant deviation from most academic publications, and I was impressed. The instrument more than justified the manual's efforts. It was gorgeous. The integration of mechanicals, layout, and electronics was like nothing I had ever seen. Hours after I fixed the thing, I continued to probe and puzzle through its subtleties. A common-mode bootstrap scheme was particularly interesting; it had direct applicability to my lab work. I resolved to steal the techniques for reducing input current and noise.

Over the next month, I found myself continually drifting away from my research project to take apart test equipment and see how it worked. The practice, alone, was interesting, but what I really wanted was to test my understanding of a piece of equipment by having to fix it. Unfortunately, Fluke, Hewlett-Packard, Tektronix, and the rest of that ilk had done their work well; the stuff didn't break.

I offered free repair services to other labs that would bring me instruments to fix. I had few takers. People had repair budgets and were unwilling to risk their equipment to my unproven care. Finally, in desperation, I paid people, in standard MIT currency (Coke and pizza), to deliberately disable my test equipment so I could fix it.

A few of my students became similarly hooked, and we engaged in all forms of contesting. After a while, the "breakers" developed an armada of incredibly arcane diseases to visit on unsuspecting working instruments. The "fixers" countered with ever more sophisticated analysis capabilities. Various games we created took points off for every test connection made to an instrument's innards, the emphasis being on how close you could get utilizing panel controls and connectors. Fixing without a schematic was highly regarded—a macho test of analytical skill and circuit sense. Still other versions rewarded pure speed of repair, regardless of method. It was great fun. It was also a form of efficient—and serious—education.

The inside of a broken, but well-designed, piece of test equipment is an extraordinarily effective classroom. The age or purpose of the instrument is of minor concern. Its instructive value derives from several perspectives.

It is always worthwhile to look at how a designer dealt with problems using available technology—and within the constraints of cost, size, power, and other realities. Whether the instrument is three months young or 30 years old has no bearing on the quality of thought behind it. Good design is independent of technology, essentially timeless. The clever, elegant, and often interdisciplinary approaches found in many instruments are eye-opening, often directly applicable to your current design work. More important, they force self-examination and, with some luck, prevent rote approaches to problem solving (and the attendant mediocre results). The specific circuit tricks you find are certainly useful and adaptable but not nearly as valuable as studying the thought processes that produced them.

The fact that the instrument is broken provides a unique opportunity; a broken instrument (or whatever is at hand) is a capsulized mystery, a puzzle with a definite and very singular "right" answer. As a result, you are forced to measure your performance against an absolute, nonnegotiable standard. When you're finished, the thing either works or doesn't work.

The reason this scenario is so valuable is that it brutally tests your thinking process. Fast judgments, glitzy explanations, and specious, hand-waving arguments cannot be costumed as "creative" activity or true understanding of a problem. After each ego-inspired lunge or jumped conclusion, you confront the uncompromising reality that the damn thing still doesn't work. The utter closedness of this reality prevents you from fooling yourself. When it's finally over, when the box works—and you know why—then the real work begins. You get to try to fix *yourself*. Poor technique, crummy arguments, and inaccurate conclusions all demand review. It's a humbling and sometimes embarrassing process, but valuable nonetheless. You learn to dance with problems instead of trying to mug them.

No room for sloppiness

It's scary to wonder how much of this sort of sloppy thinking slips into your own design work. In that arena, the system is not closed. There is no arbitrarily right answer, only choices. Things can work, but not as well as they might if your thinking had been better. In the worst case, things work but for different reasons than you count on. This situation is a disaster and more common than might be supposed.

For me, the most dangerous point in design comes when it works. Ostensibly, this "proves" my thinking correct, which isn't necessarily the case. The luxury the broken instrument's closed intellectual system provides no longer exists. In design work, results are open to interpretation and explanation, which is a dangerous time. When a design "works" is a very delicate stage; psychologically, you are ready for the kill and, consequently, less inclined to continue testing your results and thinking. That's a precarious place to be, and you have to be careful not to get into trouble. The very humanness that drives you to solve a problem can betray you near the finish line.

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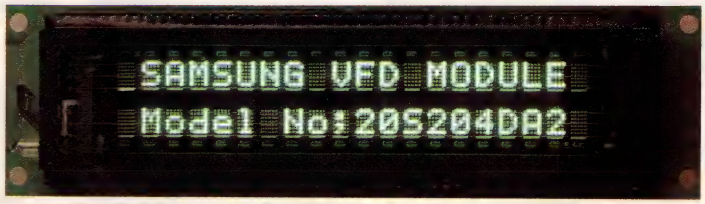

VFD MODULES

MODEL	CHARACTER FORMAT & SYMBOLS	No of Digits (Row X Column)	CHARACTER DIMENSIONS			OUTER DIMENSIONS			ELECTRICAL CHARACTERISTICS			INTERFACE				
			CH (mm)	CW (mm)	CP (mm)	L (mm)	H (mm)	T (mm)	Vcc (Vdc)	Icc (mA)	L (Typ) (ft-L)	Parallel Input	Serial Input	Self Test	Device Select	Busy Out
20S102MA4		1×20	5.0	3.5	4.7	150.0	30.0	26.6	5.0	150	200	○	○	○	○	○
20S204DA2		2×20	5.0	3.5	5.1	155.0	43.0	28.0	5.0	350	250	○	○	○	○	○
40S102MA4		1×40	5.05	3.55	4.75	240.0	40.0	30.0	5.0	350	200	○	○	○	○	○
40S201MA4		2×40	5.05	3.55	4.75	240.0	60.0	29.0	5.0	800	200	○	○	○	○	○
12L101MK1		1×12	11.4	8.7	12.5	200.0	50.0	28.6	5.0	550	250	○	○	○	○	○

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DISPLAY DEVICES

CIRCLE NO. 137

FIX IT YOURSELF!

What all this means is that fixing things is excellent exercise for doing design work, a sort of bicycle-with-training-wheels that prevents you from getting into too much trouble. In design work, you have to mix your willingness to try anything with what you hope is critical thinking. This seemingly immiscible combination can lead you to a lot of nowheres, but it can also force you to learn, which is the major reason I've been addicted to fixing since that semester back in 1968. I'm fairly sure it was Zacharias' reason for bouncing my instrument-repair allocation. I couldn't understand it then, but he had initiated me. He introduced me to what my life would become for the next 10 years. And no apprenticeship was ever more necessary, better delivered, or, years later, as appreciated.

There are, of course, less lofty adjunct benefits to fixing. You can often buy broken equipment at absurdly low cost. I once paid $10 for a dead Tektronix 454A 150-MHz portable oscilloscope. It had been systematically sabotaged by some weekend-bound calibration technician and tagged "beyond repair." The machine required 30 hours to uncover the various nasty tricks played within its bowels to ensure that it would be scrapped.

This kind of devotion highlights another benefit of fixing. There is a certain satisfaction, a kind of service to a "moral" imperative, that comes from restoring a high-quality instrument. Sure, I'll admit that this is unquestionably a gooey, hand-over-the-heart judgment, and I confess a long-term love affair with instrumentation. But, for me, it seems sacrilegious to let a good piece of equipment die.

And, finally, fixing is simply a lot of fun. I'm probably the only person at an electronic flea market who pays more for the busted stuff than for the equipment that works!

Oh boy, it's broken! Life doesn't get any better than this. EDN

▶ This article is part of Jim Williams' new book, *Another Look at Analog Circuit Design*. It will be published this spring by Butterworth-Heinemann as part of the *EDN* Series for Design Engineers. Contact (800) 366-2655 to order.

Author's biography

Jim Williams, staff scientist at Linear Technology Corp (Milpitas, CA), specializes in analog-circuit and instrumentation design. He was voted EDN's 1992 Innovator of the Year. Williams enjoys art, collecting antique scientific instruments, and restoring old Tektronix oscilloscopes.

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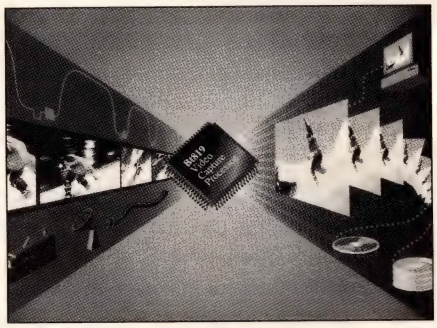
950-MHz JFET video buffer includes a 75Ω output resistor to minimize reflections. The MAX4005 has 10-pA input current, making the device suitable for high-impedance sources. Video parameters include a differential gain error of 0.11%, a phase error of 0.03°, a 60-MHz gain flatness of 0.1 dB, <3-mV offset voltage, and ≥60-dB distortion for the third harmonic. The buffer has a 1000-V/μsec slew rate, a 2-nsec settling time to 0.1%, and 350-psec rise and fall times. From $2.75 (1000). **Maxim Integrated Products**, Sunnyvale, CA. (408) 737-7600, ext 6087. **Circle No. 417**

3.3V gate-array family improves density of complex designs. The M5C series gate arrays have primary cells that contain more elements than previous generation arrays. The devices include various-sized transistors that you can use individually or in parallel to increase speed, power, and density. The core cells suit single- and dual-port RAM, flip-flops, and multiplexers. The initial offerings provide from 142,000 to 460,000 gates. A typical design using 125,000 gates in a 225-bump plastic ball-grid array or 240-lead PQFP would have an NRE charge of $125,000 and a price of approximately $65 (5000). **Motorola Semiconductor Products Sector**, Phoenix, AZ. (602) 814-4047. **Circle No. 418**

Hall-effect latches operate to 150°C. The pole of a simple ring magnet activates the A3185 and A3187 Hall-effect sensors, and the devices remain latched in the switched position until the opposite pole is applied. The devices operate from 4.5 to 24V dc and have an open-collector output that sinks 25 mA. $1.19 (1000). **Allegro MicroSystems Inc**, Worcester, MA. (508) 853-5000. **Circle No. 419**

Computer clock offers 3 and 5V operation. The Serialized Real Time Clock has an automatic sensor that detects the power-supply voltage and adjusts to the appropriate level. The clock is available as a chip (DS1688/1689) for $4.50 (1000) or as a stand-alone module (DS1691/1693) with an embedded lithium battery and crystal for $9.90 (1000). The chip can also back up and write-protect an eternal SRAM, avoiding the need to buy a separate nonvolatile SRAM. The clock chips provide counters that record the total elapsed power-on time and the total number of power-on/off cycles. **Dallas Semiconductor**, Dallas, TX. (214) 450-0448. **Circle No. 420**

High-speed data-compression chip allows modems to use 8-bit CPUs. The 9410 v.42bis compression accelerator reduces a modem CPU's workload, allowing the modem to use an 8-bit CPU. According to the company, without the accelerator, the modem must use a 16-bit CPU to achieve high throughput. The 8-bit CPU costs less, uses less power, and uses less RAM and ROM. $7 (100,000). Evaluation boards are available. **Stac Electronics**, Carlsbad, CA. (619) 431-7474. **Circle No. 421**



Video-capture processor enables integration of video capture on PC graphics systems for <$50. The Bt819 accepts analog input from TV or VCR sources and decodes and scales it for PC graphics systems. You can scale down horizontal and vertical resolution to any number of vertical lines or horizontal pixels above 1/14 of full NTSC or PAL resolution. The chip uses the company's Ultralock all-digital-video-synchronization technology. $17 (OEM qty). **Brooktree Corp**, San Diego, CA. (619) 452-7580. **Circle No. 422**

Low-power serial EEPROMs support Serial Peripheral Interface bus protocol. Offering capacities of 8 (X25080) to 64 kbits (X25642), the serial EEPROMs are configured for 5 or 2.7V operation. The devices typically

require 1 μA of standby current and 2 mA of active current at a data-transfer rate of 2 MHz. A write-protect feature lets you protect portions of the memory reserved for configuration or serialization data from inadvertent or intrusive manipulation, once the system is in operation. $2.06 (10,000) for the X25080 to $5.14 (10,000) for the X25642. **Xicor Inc**, Milpitas, CA. (408) 432-8888.

Circle No. 423

Three-pin SOT-23 μP reset eliminates external components. The μP supervisor asserts a reset signal whenever V_{cc} falls below a preset threshold. The device ignores fast transients on the V_{cc} rail, but once the device asserts a reset, it remains active for at least 140 msec after V_{cc} returns above the threshold. The available thresholds are 4.63, 4.38, 3.08, 2.93, and 2.63V. Active-low (MAX809) and active-high (MAX810) versions are available and cost $0.80 (3000). **Maxim Integrated Products**, Sunnyvale, CA. (408) 737-7600, ext 6087. **Circle No. 424**

Three multimedia video-playback chips for desktop and portable PCs. The CL-GD7542, a $39.50 (1000) LCD VGA controller for video playback, supports 800×600-pixel SVGA LCDs. The device has a dithering algorithm that eliminates color banding and contouring. The single-chip device includes a VGA controller, a frequency synthesizer, a true-color RAMDAC, and an interface for flat-panel displays. A complete video display requires two 256k×16-bit DRAMs. The CL-GD5440 $29.50 (1000) provides hardware zoom to create a 30-frame/sec, 1024×768-pixel display from video, CD-ROM, or disk input. The CL-PX4072 $35 (1000) single-chip decoder converts analog video signals from a variety of sources into digital signals. **Cirrus Logic Inc**, Fremont, CA. (510) 623-8300. **Circle No. 425**

MPEG-2-compliant decoder provides real-time decompression and expansion of color motion video. The M65770FP MPEG-2 decoder handles a full CCIR 601 702×480-pixel NTSC image at 30 frames/sec, with an image-output format of 4:2:2. The decoder complies with the MPEG-2 Main Profile at Main Level standard. The device provides a 3:2 pull-down for converting a 24-frame/sec film sequence into NTSC 30-frame/sec. It also offers pan and scan for displaying a 16:9 screen onto a 4:3 screen for digital community-antenna-TV display. The device requires two or four 4-Mbit DRAMs. It comes in a 208-pin plastic QFP and dissipates 2W from a 3.3V supply. Samples cost $500. **Mitsubishi Electronics America Inc**, Sunnyvale, CA. (408) 730-5900.

Circle No. 426

4-Mbit SRAM offers access times to 17 nsec. The EDI18L32128C SRAM has configuration controls that let you use the device as a 512k×8-bit device or as a 256k×16-bit device. The device comes in a 68-pin PLCC package and in 0 to 70 or –40 to +85°C temperature ranges. The 17-nsec version costs $234 (100). **Electronic Designs Inc**, Westborough, MA. (508) 366-5151.

Circle No. 427

Cache-data RAMs for the 486, Pentium, and PowerPC have 9-nsec access. The W73B586B and W73B601 accommodate burst-sequence addressing at 66 MHz with a 2-bit wrap-around counter. The synchronous RAMs have a

32k×18-bit organization. Other features include a 2.5-nsec setup time, a 0.5-nsec hold time, byte write capability, asynchronous output enable, and a direct interface between the processor and an external cache controller. Prices range from $35 (1000) for the 9-nsec version to $30 (1000) for the 12-nsec versions. **IC Works Inc**, San Jose, CA. (408) 922-0202.

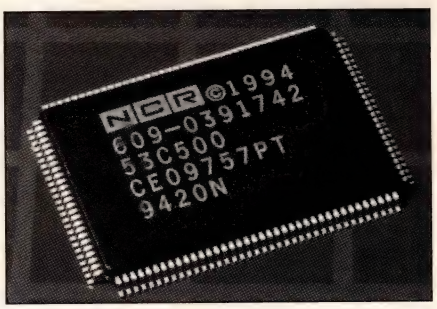
Circle No. 428

RS-232C IC has shutdown mode that reduces supply current to 1 μA. The MAX3212 monitors RS-232C receiver inputs and reduces supply current to 1 μA if no valid RS-232C level exists on the receiver inputs. The power-down mode reduces current consumption by a factor of >1000. The device has a guaranteed data rate of 230 kbps and is available in 28-pin SO and SSOP packages. From $3.29 (1000). **Maxim Integrated Products**, Sunnyvale, CA. (408) 737-7600, ext 6087.

Circle No. 429

16-Mbit flash memory in TSOP II packages suits high-density memory applications. The HN28F1600 has NOR-type nonvolatile cells, >100,000 erase/write cycle endurance, and a 512-byte sector erase. The IC offers ×8- or ×16-bit organization and has a 120-nsec access time. The relatively short access time allows random accesses directly from the flash memory instead of loading into RAM. The JEDEC-standard, 14×20-mm, 48-pin package meets high-density nonvolatile-memory requirements. Typical programming time is 10 μsec/byte or 20 μsec/8-byte page. Erase time is 10 msec/512-byte sector. The chip uses 12V for programming. $65 (10,000). **Hitachi America Ltd, Semiconductor & IC Division**, Brisbane, CA. (800) 285-1601, ext 13.

Circle No. 430



PCMCIA-SCSI controller offered as a chip or as a Type II PCMCIA card. The NCR53C500 has features to reduce power consumption, simplify connectivity, improve system integration, and maximize performance. The chip uses power and ground plane isolation of I/O pads to improve noise rejection. Power-management features include SCSI bus isolation, termination power sensing, and a power-down mode. $16.30 (1000). The NCR5000 PCMCIA card is bundled with the company's SCSI Device Management Systems (SDMS) operating-system drivers for DOS, Windows, and OS/2. $90 (1000). **NCR Microelectronic Products Div of AT&T Global Information Solutions**, Fort Collins, CO. (800) 334-5454.

Circle No. 431

Hall-effect sensors communicate over two-wire bus. The A3054KU and A3054SU Hall-effect sensors are

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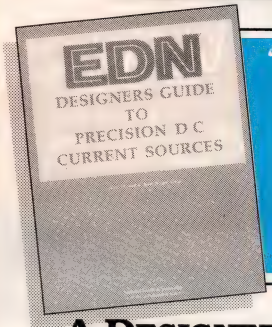

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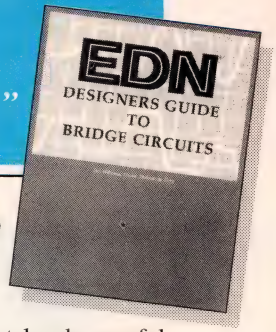

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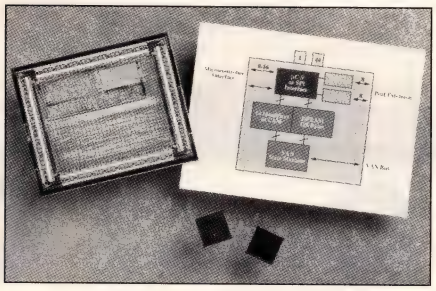
NEC

CIRCLE NO. 31

digital magnetic-sensing devices for multiple-sensor systems that communicate over a two-wire power and signal bus. The devices use a factory-programmed sequential-addressing scheme. Each IC responds to a signal on the bus and returns the IC's own diagnostic status and the status of each monitored external magnetic field. Up to 30 sensors can use the same two-wire bus. From $1.35 (1000). **Allegro MicroSystems Inc**, Worcester, MA. (508) 853-5000. **Circle No. 432**

RAMDAC with zoom and filter enlarges video to full screen and full motion. The W30C516 ZOOMDAC has a 2-D tracking filter that removes jagged zoom artifacts and displays video images at up to 1280×1024-pixel resolution with 16 bits of color. The device can also display 24-bit color at 800×600 pixels. $15 (10,000). **IC Works Inc**, San Jose, CA. (408) 922-0202. **Circle No. 433**



Data-link controller complies with the Vehicle Area Network (VAN) standard. The 29C462 IC handles all module and message types the VAN protocol specifies. Compatible with architectures from Intel and Motorola, the controller can be used in Controller Area Network (CAN) sockets with a simple change in line driver and software. The controller handles communication with master, slave, or synchronous modules. In a 44-pin PLCC, $6 (low volumes). **Temic**, Santa Clara, CA. (800) 554-5565, ext 42. **Circle No. 434**

95%-efficient synchronous step-down controllers deliver 10A at 2.5 to 6V. The MAX796-799 family step-down controllers work with external n-channel MOSFET power switches and accept a 4.5 to 30V input. The controllers have an idle mode that consumes 675 µA at 3.3V and a shutdown mode that consumes 1.2 µA. From $3.65 (1000). **Maxim Integrated Products**, Sunnyvale, CA. (408) 737-7600, ext 6087. **Circle No. 435**

Flexible MVIP interface circuit has a 384×384-switch matrix. The MT90810 complies with the Multi-Vendor Integration Protocol (MVIP), a standard call-processing architecture. The switch suits distributed switching, voice and data multiplexing, computer-telephony, and multimedia applications. The local serial interface is programmable to 2.048, 4.096, or 8.192 Mbps. Digital and analog PLLs provide rapid recovery in case of network failures. Available in a 100-pin PQFP, the IC costs $25 (10,000). **Mitel Semiconductor Corp**, Kanata, ON, Canada. (613) 592-2122. **Circle No. 436**

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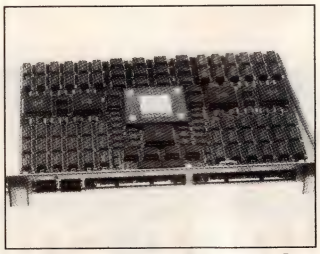
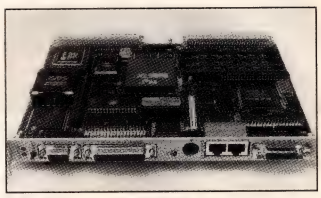
Stand-alone multiprocessor DSP boards offer up to 500-MFLOPS performance. The Puma board uses three ADSP21020 DSP chips, and the Panther uses five of the chips. Both products can connect with a host computer via an RS-232C interface. Interprocessing communications among the DSPs is via 2k×32-bit dual-ported shared-memory blocks using interprocessor interrupts. Each processor has its own 512-kbyte EPROM boot memory, 128k×48-bit, zero-wait-state program memory, and 128k×32-bit, zero-wait-state data memory. Nonvolatile RAM stores system-configuration data when the system powers down. IXI mezzanine modules can provide a variety of A/D, D/A, and digital interface functions. Puma starts at $5000, and Panther starts at $14,500. **BittWare Research Systems**, Concord, NH. (603) 226-0404. **Circle No. 350**



VMEbus board provides vector and scalar operations in high-speed, real-time DSP systems. The VSP-9 uses a Sharp LH9124 vector processor and a TI TMS320C40 scalar processor, both operating at 40 MHz. The board performs continuous 1024 complex FFTs in 80 µsec each. Streams of 64k complex FFTs require 8.3 msec each. FIFO-buffered input and output parallel ports on the board's front panel are each 48 bits wide and accommodate a complex data stream or two real streams at 40M words/sec. The front panel has two 8-bit, 20-Mbyte/sec FIFO-buffered 320C40 communication ports for data transfer among 320C40 devices on other boards. $13,678. **Pacific Cyber/Metrix Inc**, Dublin, CA. (510) 829-8700. **Circle No. 351**

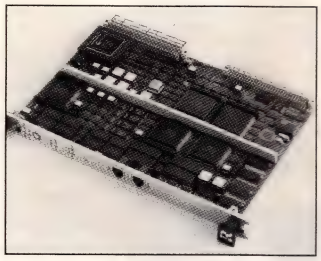
PowerPC CPU board for military VMEbus applications. The PMV68 CPU-601 power processor is a single-width, 6U VMEbus board that is compatible with VME64, IEEE 1014-1987, and IEEE 1101.2-1992 specifications. The board uses a 50-MHz PowerPC 601 CPU and is available with 16 to 64 Mbytes of DRAM. A 64-bit VMEbus interface and a VSB interface are available. Other features include 4 Mbytes of flash EPROM, 2 kbytes of serial EEPROM, and two RS-423 ports. The board is available for benign, rugged, and mil-spec applications. From $6000. **Radstone Technology Corp**, Montvale, NJ. (201) 391-2700. **Circle No. 352**



VMEbus CPU boards use 80486 processor. The VMIVME-7487 uses an Intel 80486 CPU and is compati-

ble with PC/AT software. The board accepts one bank of 32-bit-wide DRAM with a maximum capacity of 16 Mbytes. Onboard DRAM is dual-ported to the VMEbus. The board includes a video interface, a floppy-disk-drive controller, and an IDE controller. From $2315. The VMIVME-7489 also uses the 80486 CPU and is compatible with PC/AT software. The board accepts PC/104 modules, has an optional cache memory, provides up to 32 Mbytes of DRAM, has floppy-disk and IDE controllers, and has two serial ports. From $2262. **VME Microsystems International Corp**, Huntsville, AL. (205) 880-0444. **Circle No. 353**

VME64 bus FDDI controller has P2 I/O connections. The FDDI-1P Fiber Distributed Data Interface (FDDI) controller board provides connections via a P2 transition module that accommodates fiber and copper transmission lines. The P2XF optical transition module provides MIC and ST optical connections and TP-PMD twisted-pair copper



connections. The board simultaneously supports 100-Mbps network access, high-speed VME data transfers, and on-board network-protocol processing. From $4295. **Radstone Technology Corp**, Montvale, NJ. (201) 391-2700.

Circle No. 354

Serial programmer for the 68HC11 microcontrollers. The SPGMR11 68HC11 serial programmer is a single-device programmer that operates either connected to a PC or in series with the company's 68HC11 Modular Development System (MMDS11). The modular design of the programmer lets it program all 68HC11 family devices and package types. The unit costs $250, and programming adapters start at $120. **Motorola Microcontroller Technologies Group**, Austin, TX. (512) 891-3465.

Circle No. 355

486-based, single-board computer offers fast GUI performance and PC/104 expansion. The SBC104-DX is available with a range of processors, from a 25-MHz 486SX to a 100-MHz 486-DX4. The board has local-bus video and a local-bus IDE hard-disk-drive interface. The combination provides a fast graphical user interface (GUI) engine in a 5×6.5-in. board. A Windows accelerator is built in. The board supports 1024×768 and 640×480 TFT LCDs. Space for 16 Mbytes of DRAM is available on board. Power consumption is less than 8W. From $1895 with 4 Mbytes of DRAM. **Computer Dynamics**, Greer, SC. (803) 877-8700.

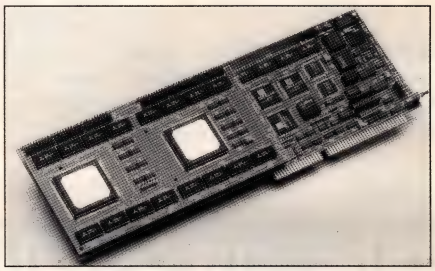
Circle No. 356

Embedded VMEbus PC has high-performance video and Ethernet onboard. The VME-2486 Embedded PC is available with an 80486DX processor running at 33, 66, or 100 MHz. The board has accelerated local-bus video with

256 colors at resolutions of up to 1280 ×1024 pixels, a 10Base2 (Thinwire) Ethernet interface, a jumperless board configuration, and an ISA bus expansion interface. The board comes with 4, 8, 16, or 32 Mbytes of shareable DRAM. Other features include floppy, IDE, and SCSI-2 interfaces; two serial ports; a parallel port; and a keyboard port. From $3400 (100). **Logical Design Group Inc**, Raleigh, NC. (919) 851-1101.
Circle No. 357

High-bandwidth OSF/1 DEC Alpha AXP to VMEbus interface board. The Model 497 TURBOchannel to VMEbus board and Model 954 OSF/1 support software connect an Alpha system to a VMEbus system with copper cable up to 25 ft. Fiber-optic cabling optionally increases the distances to 2000m. The board provides a memory-mapped interface between the two buses with bidirectional bus mastership. Two modes of DMA are available. The DMA controller can move blocks of data up to 16 Mbytes between the systems at speeds of 26 Mbytes/sec. A slave-DMA mode allows a VME card with a DMA controller to DMA into Alpha system memory as though it were VMEbus memory. The board costs $2850, and the software costs $600. **Bit 3 Computer Corp**, Minneapolis, MN. (612) 881-6955. **Circle No. 358**

Single-board VME bus computer has 32-MHz 68040 CPU and IndustryPak interface. The MVME162 has an IndustryPak interface with multispeed DMA capability that complies with the emerging ANSI specification covering DMA and 32-MHz operation. The board accommodates up to 32 Mbytes of RAM. From $2045. **Motorola Computer Group**, Tempe, AZ. (602) 438-3287. **Circle No. 359**



Quad-DSP board for ISA or EISA provides parallel processing for $1795. The MZ 7914 uses four TMS320C44 processors operating at 50 MHz to deliver 200 Mflops. Each board accommodates up to 40 Mbytes of SRAM that you can configure in a Harvard-style memory architecture. The board is intended for real-time image processing, telecommunications, and other high-performance DSP applications. A suite of development tools to aid in the development of parallel processing applications is available. The board will be available this quarter and is subject to availability of the processor. **Mizar Inc**, Carrollton, TX. (214) 277-4600. **Circle No. 360**

Image-management software for entry-level applications. Frequent Filer Version 3.0 provides multiple-page display, complex annotation capabilities, built-in optical-character recognition, and an optional full-text retrieval engine. The product has a single-level database that works with a variety of SQL database servers. Direct indexing emulates a document-oriented filing system, making it easy to build and

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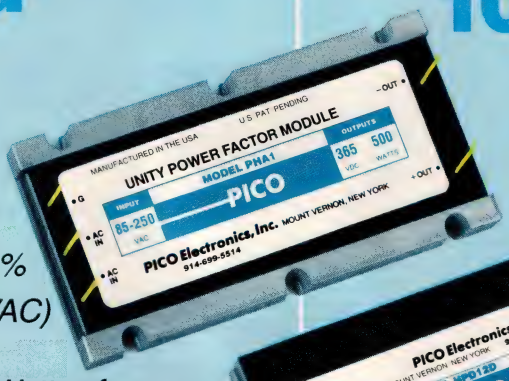

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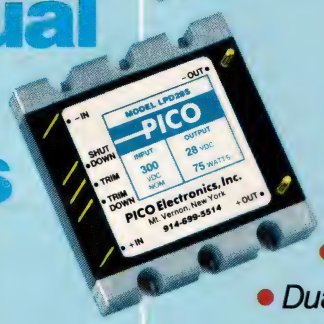

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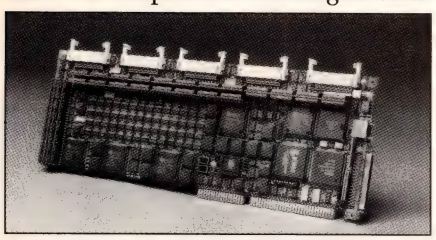
CIRCLE NO. 123

deploy imaging applications. The software starts at $600 per seat. **Optika Imaging Systems Inc**, Colorado Springs, CO. (719) 548- 9800.
Circle No. 361

200-Mflops DSP-based signal-processing board has wideband I/O capability. The AP85c ISA bus board has five TMS320C31 40-MHz DSP chips arranged in a master-slave configuration with all processors acting as com-



putational peers. The master processor controls most of the I/O capability, including an 80-Mbyte/sec bidirectional FIFO port for use with external devices, an RS-232C port, and a 20-Mbyte/sec SCSI-2 port. Each of the four slave processors has an 80-Mbyte/sec bidirectional expansion port. The board supports a maximum of 16 Mbytes of global memory and 3 Mbytes of local SRAM. $8995 with 4 Mbytes of memory. **Analogic Corp**, Peabody, MA. (508) 977-3000. **Circle No. 362**

DSP board for Micro Channel architecture. The Elf/MC DSP platform has a TMS320C31 floating-point DSP, a stereo 16-bit A/D and D/A, and 256k words of DRAM. The board includes a digital audio interface and a daughterboard connector for use with the company's Elf add-on boards. The Micro Channel board costs $1495, and development systems start at $3295. **Atlanta Signal Processing Inc**, Atlanta, GA. (404) 892-7265. **Circle No. 363**

Capacitive touch screen for Compaq ProLinea Net1/25s. The TruePoint ProLinea system is a combined touch monitor and PC for kiosk and multimedia developers who are looking to get touch applications to market. The system comes standard with an Intel 486SX/25 processor, 1 Mbyte of RAM expandable to 20 Mbytes, and one 1.44-Mbyte floppy-disk drive. The device provides a graphic resolution of 1024×768 and a touch-screen resolution of 1024×1024. The system is available in both Ethernet NIC and token ring NIC versions. List price is $2725. **MicroTouch Systems Inc**, Methuen, MA. (508) 659-9000.
Circle No. 364

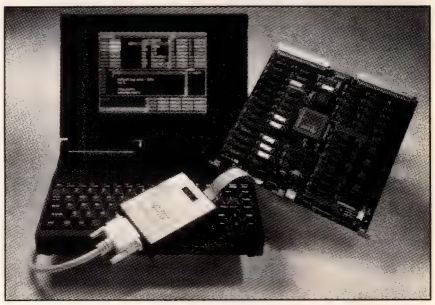
Graphical data-analysis software package collects and analyzes technical data. The DADiSP/AdvDSP 1.0 add-on module is a digital signal-processing module integrated with the company's DADiSP worksheet. The module provides a variety of DSP algorithms, including advanced FFT analysis, power-spectral-density estimation, digital interpolation, and cepstrum analysis. Each routine is available via a simple fill-in form menu and as a direct command line function. $495 for PCs and $995 for workstations. **DSP Development Corp**, Cambridge, MA. (617) 577-1133. **Circle No. 365**

Digital audio board for PCs provides real-time ISO/MPEG Layer I/II encoding. The Model Z1e 16-bit broadcast quality, stereo-sound board uses the TMS320C31 DSP to deliver compression rates as high as 12:1 at 44.1-kHz sample rates. The board also provides other compression formats, including Microsoft and IMA ADPCM. Performance specifications include a THD+N of 0.06%, a dynamic range of 85 dB, and a frequency response of 20 Hz to 20 kHz. $595. **Antex Electronics Corp**, Gardena, CA. (310) 532-3092.

Circle No. 366

i960-based single-board computer has dual-memory architecture. The CVME964 uses a dual-memory architecture to avoid the problem of the processor and DMA controller competing for the same memory resource. The condition, known as starve out, is avoided by having a private memory for the processor and a global or packet memory for the I/O devices and processor to share. The private memory can store code, especially interrupt service routines, stacks, and variables. The shared memory is used for I/O buffers and packet storage. The VME board with 2 Mbytes of private memory and 8 Mbytes of shared memory costs $3030 (100). **Cyclone Microsystems**, New Haven, CT. (203) 786-5536.

Circle No. 367



Nonintrusive emulator for the TMS320C3x floating-point DSPs. The EMU320C3X is a scan-path emulator that provides full-speed emulation, including access to all memory and internal DSP registers. The emulator connects to a PC's bidirectional parallel port and runs from an 8- to 16-Vdc power supply, suiting it for portable work in automotive, avionics, or field service. The system is compatible with 3 and 5V DSPs. $2999. **Spectrum Digital Inc**, Sugar Land, TX. (713) 561-6952.

Circle No. 368

Software-development kit for intelligent PCI I/O applications. The i960 Processor PCI I/O software-development kit gives developers of intelligent peripheral-component-interconnect (PCI) bus I/O cards the ability to start immediate development of software in an environment similar to that in which the PCI I/O add-in card product can operate. The basic development kit costs $960, and I/O modules are available: Ethernet, $408; SCSI-2, $512; SCSI-3, $680; and high-speed serial, $325. **Intel Embedded Processor Division**, Chandler, AZ. (800) 628-8686.

Circle No. 369

Daughtercards for 6- and 12-processor DSP boards. The AUX1 ($3000) and AUX2 ($4500) daughter-

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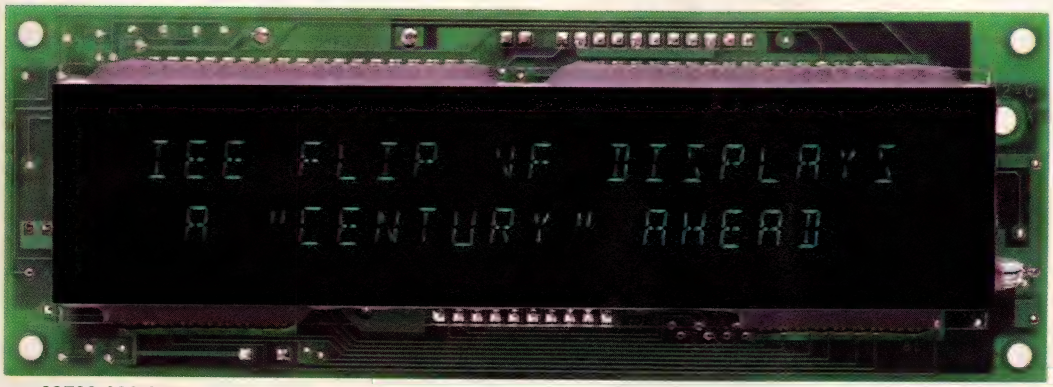

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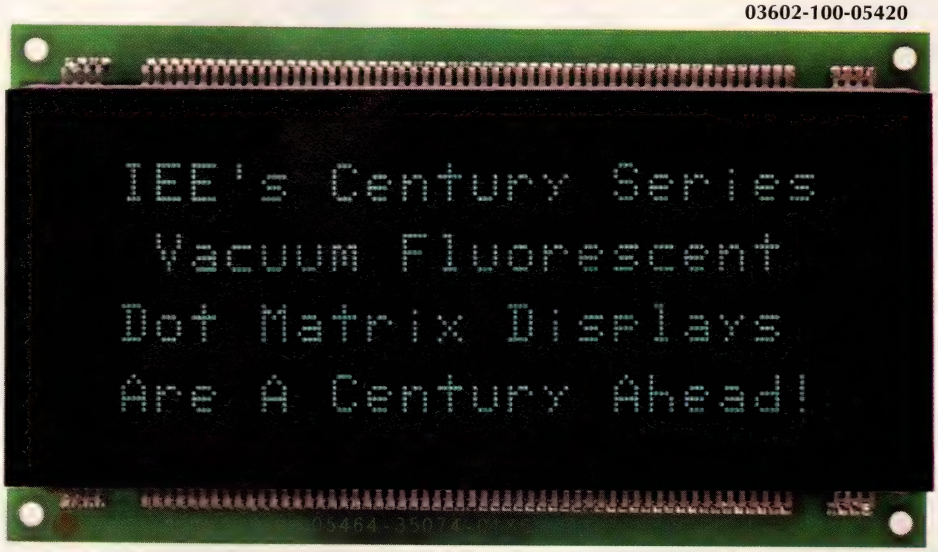

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Model	Character Format	Display Format	Character Height	Package Size: Length	Width	Depth	Max. Current
03602-100-05420	5x7 dot matrix	4x20	5mm	5.00″	2.78″	0.92″	890mA
03602-105-05220	5x7 dot matrix	2x20	5mm	5.00″	2.25″	0.88″	405mA
03602-122-09220	5x7 dot matrix	2x20	9mm	7.75″	2.58″	1.00″	675mA
03602-124-09420	5x7 dot matrix	4x20	9mm	7.75″	3.40″	1.00″	1300mA
03702-020-05220	14-segment	2x20	5mm	5.65″	1.98″	0.82″	270mA
03702-021-08110	14-segment	1x10	8mm	5.00″	1.60″	0.90″	140mA
03702-022-13112	14-segment	1x12	13mm	7.20″	2.40″	0.90″	323mA
03702-024-09116	14-segment	1x16	9mm	6.70″	2.30″	0.90″	360mA
03702-026-09120	14-segment	1x20	9mm	8.30″	2.35″	0.95″	390mA
03702-029-13120	14-segment	1x20	13mm	10.20″	1.93″	0.96″	526mA

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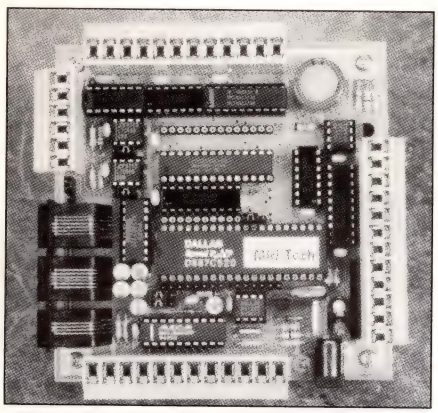
cards add one or two AT&T DSP32C processors with stereo codec dedicated to each processor. The HC12 mezzanine module ($4000) has six stereo codecs, providing 12 audio I/O channels via 16-bit A/D and D/A converters. The 6UAES/422 mezzanine card ($1500) supports digital proaudio I/O, based on the Audio Engineering Society/European Broadcast Union (AES/EBU) and Sony/Philips Digital Interface Format (S/PDIF) standards. The daughtercards are designed for the VME6U6 board containing six AT&T DSP32C processors ($8900) and the VME9U12 with 12 processors ($17,000). **Communication Automation & Control Inc**, Allentown, PA. (610) 776-6669. **Circle No. 370**



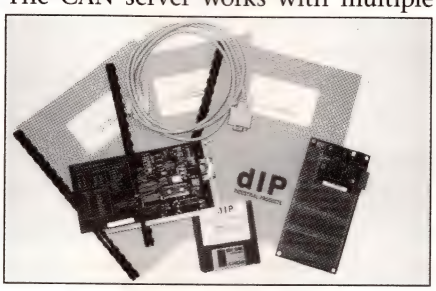
8031 code-compatible single-board computer operates at 8 MIPS. The ec.52 SBC is based on the Dallas Semiconductor DS87C520 and operates at 33 MHz. The board comes with 16 kbytes of EEPROM, 1 kbyte of data RAM, and 32 kbytes of nonvolatile high-speed program/data RAM. The I/O includes eight digital inputs and outputs and a 12-bit, eight-channel A/D. Two high-speed UARTs provide two channels of RS232C or RS485 communication. The SBC starts at $240. The PC-hosted development tools, consisting of a simulator, debugger, and cross-assembler, cost $49.95. A C language developer's kit costs $99.95. **Mid-Tech Computing Devices**, Stafford, CT. (203) 684-2442.
Circle No. 371

486-based PC/AT local-bus single-board computer accommodates up to 32 Mbytes of DRAM. The VIPer880 family of SBCs is available with 486 processors from the 486SX-25 ($1300) up to the 486DX4 operating at 100 MHz. The board comes with on-board local-bus SVGA; SCSI, IDE, and floppy-disk controllers; and two serial and one parallel port. You can configure the device with 1 Mbyte of bootable flash EEPROM and 512 kbytes of SRAM. The PC/104 mezzanine bus provides expansion. **Teknor Microsystems Inc**, Boisbriand, PQ, Canada. (514) 437-5682. **Circle No. 372**

PowerPC systems available with Windows NT. The PowerStack family of client/server and multiuser computer systems based on the PowerPC 603 and PowerPC 604 μP are available with Windows NT 3.5. The model E603-66P with 16 Mbytes memory, 1-Gbyte disk, and CD-ROM costs $5995. A similarly configured E604-100P starts at $7995. **Motorola Computer Group**, Tempe, AZ. (800) 624-6449. **Circle No. 373**

Compilers and graphics package for OS/2 on Pentium-based systems. The NDP OS/2 developer's package provides a Fortran, C/C++, or Pascal compiler; the IBM OS/2 Toolkit; and the IBM WorkFrame. The compilers come with MGX, the company's device-independent, vector-based graphics and plotting package. The package costs $895. **Microway**, Kingston, MA. (508) 746-7341. **Circle No. 374**

Windows DDE servers let you access data from CAN-based devices. The QuickCAN servers are compatible with Micro Switch SDS, Allen-Bradley DeviceNet, and Philips 82C150 CAN-based area networks. Any Windows DDE client application, such as Excel, Visual Basic, etc, can communicate with the servers and access the same data. Clients can communicate simultaneously with the CAN devices. The CAN server works with multiple



devices having up to 32 input and output points and supports independent scan rates for each device. The server costs $395. A CAN-evaluation hardware kit costs $295. **DIP Industrial Products Inc**, Moreno Valley, CA. (909) 924-1730. **Circle No. 375**

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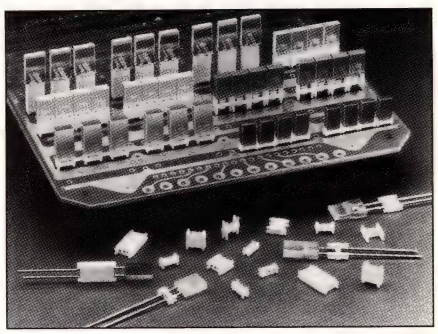
Polypropylene film capacitors suit high-voltage snubbing and SCR commutation applications. The PWS 100°C polypropylene capacitors with metal foil are available in capacitance ranges from 0.001 to 0.47 µF. Voltages ranges are 630 to 2000V dc and 300 to 500V ac. The capacitor family has a dV/dt range of 1800 to 27,000 V/µsec. From $0.27 (1000). **Illinois Capacitor Inc**, Lincolnwood, IL. (708) 675-1760. **Circle No. 394**

SAW voltage-controlled oscillator suits SDH/SONET or STM systems. The CMS1000 series of 130- to 2600-MHz custom voltage-controlled oscillators suits synchronous-digital-hierarchy/synchronous-optical-network and STM systems. A surface-acoustic-wave (SAW) delay line stabilizes the output frequency, which is adjustable up to 1000 ppm. Supply voltage ranges from –5.2 to +12V, and packaging is hermetically sealed. Price range is DM300 to DM600 (10,000). **C-MAC Quartz Crystals**, Harlow, UK. (44) 279 626626. **Circle No. 395**

$99 IR thermocouple has –50 to +550°F range. The IRt/c.01 noncontact thermocouple overcomes the problems of contact thermocouples, such as vibration, sterility, corrosion, drift, and contact error. The 1.28×0.71-in.-diameter device meets all NEMA standards and is hermetically sealed in an ABS case. The sensor has an 80-msec response-time constant and standard J, K, E, or T outputs. **Exergen Corp**, Newton, MA. (617) 527-6660. **Circle No. 396**

Signal connector with fully isolated contacts carries 5A on a 3-mm grid. The Micro-Fit 3.0 connector system uses phosphor-bronze box-type crimp-receptacle terminals that accept 20- to 30-AWG wire and provides four points of contact. The connector is available in circuit sizes of 2 to 24. Vertical or right-angle headers are available for through-hole and true surface-mount-technology (SMT) versions. Full polarization on both sides of the connector helps prevent accidental mismating, and positive latching helps prevent accidental disconnection. A 10-circuit vertical header in an SMT-version costs $1.083 (1000). **Molex Inc**, Lisle, IL. (708) 969-4550. **Circle No. 397**

Metalized-polyester film capacitors suppress interference. The Type 914X film capacitors have UL, CSA, and VDE safety approvals. They are encapsulated in a flame-retardant (UL 94V-0) epoxy resin. The capacitors are noninductive, self-healing, and moisture-resistant. The capacitors have a –25 to +85°C operating-temperature range and standard tolerances of ±10 and ±20%. Dissipation factor is <1% at 1 kHz, and capacitance range is 0.0047 to 0.22 µF. Voltage ratings are 125 and 250V ac. $0.12 (1000). **Tecate Industries Inc**, El Cajon, CA. (619) 448-4811. **Circle No. 398**



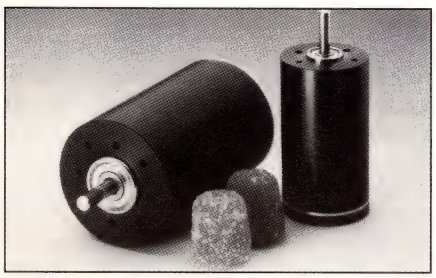
Self-retaining mounts for rectangular LEDs are auto-insertable. The RL Series molded mounts accept two- and three-lead rectangular LEDs and provide accurate and uniform positioning and protection during assembly and handling. The mounts accept 2×4- or 2×5-mm LEDs and are symmetric for placement onto leads without orientation. Manufactured from nylon, they are available with elevations from 0.060 to 0.740 in. Typical price is $44.50/1000 (10,000). **Bivar Inc**, Irvine, CA. (714) 951-8808. **Circle No. 399**

Ultrafast switching IGBTs have low switching and conduction losses. The HGTP20N60B3 (in TO 220 package, $3.45 (1000)) and the HGTG-20N60B3D with an antiparallel diode from emitter to collector (in TO 247 package, $6.43 (1000)) are N-type insulated-gate bipolar transistors (IGBTs). They have 140-nsec typical fall times

for switching large currents in power circuits, enabling the use of 200-kHz switching frequencies. The 600V IGBTs are rated for 40A continuous at 25°C and 20A at 110°C. **Harris Semiconductor**, Melbourne, FL. (800) 442-7747, ext 7281. **Circle No. 400**

Power-supply-styled enclosures are available in 30 configurations. The PS Series power-supply-styled enclosures are available in desktop, two-pole, and three-pole (grounded), 15A, 120V-ac configurations. You can specify bases with an integral hold-down tab to semipermanently secure the unit to a wall receptacle. A recessed smooth area is standard on all bases for labels, coding, or printing. Bases also have internal mounting bosses for pc-board screw-down mountings. From $2.53 (1000). **Polycase Products**, Cleveland, OH. (216) 391-2891. **Circle No. 401**

Chip resistors offer high voltage ratings. Surface-mount chip resistors incorporating the vendor's fine-line technology offer 0805-size resistors with 500V ratings and 2512-size resistors with a 2500V rating. Wrap-around, flip-chip, and wire-bond configurations are also available. From $0.40 to $4 (1000). **Ohmcraft Inc**, Pittsford, NY. (716) 586-0823. **Circle No. 402**



Miniature brushless dc servomotors provide high power in small packages. The BL1 and BL2 servomotors provide a maximum power of 85W. The motors use rare-earth magnets and have outside diameters of 24 and 35 mm. According to the company, the patented System Faulhaber coils provide smooth operation at low speeds and reliability in severe environments at speeds up to 40,000 rpm. All motors in the series have preloaded ball bearings and operating ranges to 125°C. From $140 (5000). **Micro Mo Electronics Inc**, St Petersburg, FL. (813) 822-2529. **Circle No. 403**

Pressure sensors provide 4.5V span from 5V supply. The ASCX series pressure sensors have a typical maximum output of 4.75V at full-scale pressure and are available in absolute, differential, and gage pressures from 1 to 150 psi. The sensors provide convenient signal levels for electronic circuitry without requiring buffer amplifiers and level shifters. Offsets may be adjusted externally. The sensors have low quiescent current levels making them suitable for battery power applications. Response time is 100 μsec. $30 (100). **SenSym Inc**, Milpitas, CA. (408) 954-1100. **Circle No. 404**

Small, ovenized crystal oscillator combines high stability, low power, and quick warmup. The OX-0017 crystal oscillator uses direct heating and direct thermal sensing of the central crystal, eliminating the need for an internal oven. The oscillator measures 35.8×27.5×16 mm and consumes 2.7W. The crystal is stress-compensated to withstand continual high temperature and is available in frequencies from 8 to 20 MHz. Standard frequencies are the 900-MHz derivatives for telecommunications, including 8.192, 10, and 15.84 MHz. Standard stability is ±0.01 ppm over –20 to +70°C. Stability to ±0.001 ppm is available. From $200 (1000). **Raltron Electronics Corp**, Miami, FL. (305) 593-6033. **Circle No. 405**

N-channel enhancement-mode MOSFET in SOT-23 package offers 1V gate-threshold voltage. The TN2101K1 low-threshold MOSFET features a drain-to-source breakdown voltage of 15V and a drain-to-source on-resistance of 7Ω max at V_{GS}=3V and I_D=50 mA. On resistance is 50Ω at V_{GS}=1.2V and I_D=2 mA. From $0.27 (1000). **Supertex Inc**, Sunnyvale, CA. (408) 744-0100. **Circle No. 406**

Family of TVS diodes for high-speed data lines in LANs and wide-area networks. The LCDA series of transient-voltage-suppressor (TVS) diodes protects sensitive circuits and ICs from overvoltage from ESD, lightning, and inductive load switching. The diodes add a 5-pF max capacative load per line and respond in <1 psec.

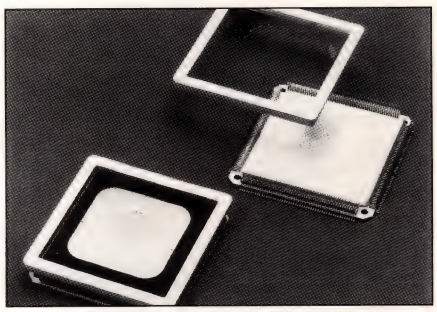
The devices meet the ESD-transient-immunity requirements of the IEC 801-02 standard for ESD with a peak >25 kV and meet all threat levels of the IEC 801-4 standard for electrical fast transients. The devices have a transient power rating of 300W and are available in standoff voltages of 5, 12, 15, and 24V. $2.60 (5000). **Semtech Corp**, Newbury Park, CA. (805) 498-2111.

Circle No. 407

Read/write RFID tags facilitate portable databases. The RF-identification (RFID) reader/writer reads or writes the 256-bit memory of ID device tags. The read/write RFID tag measures 0.4×0.8 in. Depending on the tag and reader configuration, read and write distances can range up to 11.5 in. The passive tags require no batteries and provide an infinite number of reads and greater than 100,000 write operations. The reader/writer interfaces to a host computer through an RS-232C interface and costs $695. The tags sell for $9.95. **Hughes Identification Systems**, Tustin, CA. (714) 573-7294.

Circle No. 408

Ultraminiature tactile momentary-switch family offers 14 models. The MJTP tactile-switch family includes through-hole and surface-mount, single-pole switches that use a snap-dome construction. The switches are available with vertical and right-angle mounts, with and without grounding tabs, in high- and low-profile packages, and with round or square actuators. Models with LED illumination are also available. Contact ratings are 50 mA at 12V dc. All models have a dielectric-withstand voltage rating of 250V ac for one minute. Typical sizes are 0.125 in. wide×0.25 in. long×0.25 in. high and 0.25 in. wide×0.25 in. long×0.063 in. high. From $0.09 (10,000). **Mors/Asc**, Wakefield, MA. (617) 246-1007. **Circle No. 409**



Low-profile surface-mount PQFP socket. The 208-position Micro-Pitch socket for JEDEC-approved PQFPs includes a cover to ensure chip retention. According to the manufacturer, the device helps reduce import tariffs, which simplifies servicing, eases processor upgrading, and avoids heat damage to chips during soldering. From $5.27 in quantity. **Amp Inc**, Harrisburg, PA. (800) 522-6752.

Circle No. 410

SMT sockets for Dallas Semiconductor nonvolatile RAM devices. The sockets allow mounting of nonvolatile RAMs after reflow soldering, protecting the lithium power source from heat damage. The sockets have an above-board profile of 0.175 in., an integrated pick-and-place tab, and 100%-inspectable solder joints. The

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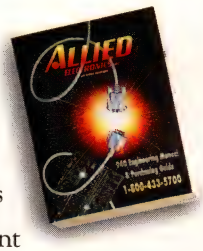

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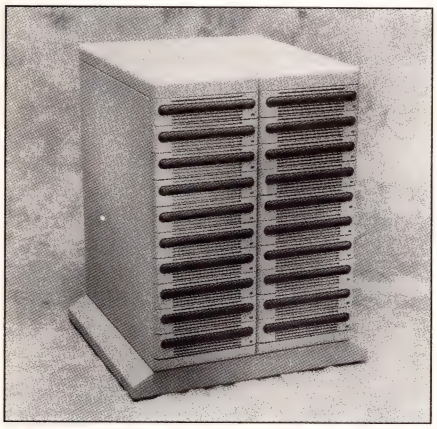
sockets are available in 26- and 34-pin versions from $0.74 (10,000). **McKenzie Technology**, Fremont, CA. (510) 651-2700. **Circle No. 411**

Surface-mount inductors have high current capability. The IHSM-4825, IHSM-5832, and IHSM-7832 have inductance values from 1 to 18,000 μH and dc ratings to 9A for the lower inductance values. The inductors suit EMI/RFI suppression in power applications, particularly in dc/dc converters. Typical price for a 1-μH inductor with an 8.6A current rating is $1.50 (1000). **Dale Electronics Inc**, Columbus, NE. (402) 563-6350. **Circle No. 412**

Toroid mounts separate windings from the horizontal mounting surface. These common-mode toroid mounts separate the windings and the insulation of a toroid when mounting to a pc board or chassis. The mounts suit use in toroidal common-mode chokes and provide standoffs to allow solder-fillet formation and flushing solder-flux residues. The mounts are available in 20 incremental sizes and feature cored-countersunk holes to assist in feeding leads. From $0.25 to $0.60 (1000), depending on size. **Robison Electronics Inc**, San Luis Obispo, CA. (805) 544-8000. **Circle No. 413**



RAID-ready desk-side storage enclosure has large capacity. The two-column×10-row redundant-array-of-individual-disks (RAID)-ready enclosure holds 20 half-height modules in two columns or 10 full-height drive modules. The enclosure features hot-swappable, removable modules that include a power supply for each drive. As an option, the vendor can integrate the CMD CRD 5000 RAID controller. From $2170. **Trimm Industries**, North Hollywood, CA. (818) 764-9500. **Circle No. 414**

Zero-insertion-force socket for Intel OverDrive processor. The 237-pin ZIF 97000-2010 socket meets the specification for the upgrade socket Intel designates as Socket 3. The 19×19-array socket is molded in a liquid-crystal polymer that enables it to withstand the temperatures of any solder-reflow process. Integrally molded tabs on the body of the socket allow for heat-sink attachment directly to the socket via a heat-sink clip. Indents in the surface of the socket also allow clipping a heat sink to the body of the inserted device. $2.25 (OEM qty). **McKenzie Technology**, Fremont, CA. (510) 651-2700. **Circle No. 415**

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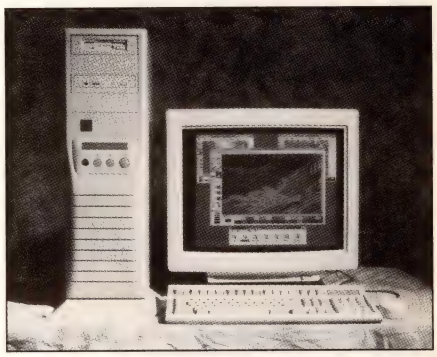
PLC-compatible, eight-channel ADC card. The EH-94300 has eight channels of 4- to 20-mA input with 12-bit resolution. PLC inputs and outputs are optoisolated to 3500V. The 3.2-in.-wide×5.3-in.-long card snaps into a standard DIN card rail and operates from 24V dc. Three-state data and control inputs allow multiple ADC cards to connect to one PLC port card. $620. **EH Engineering Ltd**, Lincoln, NE. (402) 466-6720. **Circle No. 377**

Dual-channel SCSI boards for VESA and EISA buses connect 14 peripherals. The dual-channel ABP752 EISA bus SCSI board provides a 20-Mbyte/sec data-transfer rate. The ABP852 dual-channel SCSI board for the VESA bus offers a 10-Mbyte/sec data-transfer rate. Both SCSI boards come with Corel's SCSI Version 2 drivers and cost $479. The company also provides the boards with Corel's network manager, RAID (Level 4 and 5), and Jukebox software for $699. **AdvanSys**, San Jose, CA. (515) 752-5359. **Circle No. 378**

Two-channel analog-output card for PCMCIA has 12-bit resolution. The PCM-DAC02 is a Type II PCMCIA card with voltage ranges of 0 to 5, 0 to 10, ±5, and ±10V. The card also provides eight bidirectional digital I/O lines. An optional PCM-TERM15 screw terminal box connects to the module with an attached 10-in. cable and accepts 12- to 22-AWG wires. $249. **ComputerBoards Inc**, Mansfield, MA. (508) 261-1123. **Circle No. 379**

VMEbus audio processor implements ISO MPEG-1 audio-compression algorithm. The MPEG digital audio processor, a single-slot, double-VMEbus board, compresses mono and stereo signals. You can adjust the compression ratio over a wide range, delivering sound quality from high-fidelity CD level down to approximately "toll" telephone quality. The audio processor can encode and simultaneously decode for monitoring, and it has digital and balanced-analog audio inputs and outputs. It operates at any of the valid MPEG-1 audio sampling rates: 32, 44.1, or 48 kHz. A sample-rate converter allows digital audio input at one rate to be encoded at another rate. $4295. **Atlanta Signal Processing Inc**, Atlanta, GA. (404) 892-7265. **Circle No. 380**

Sunlight-readable, flat-panel VGA monitor. The Deeco Systems ST1230-SR VGA monitor uses a backlit transreflective LCD with 640×480 resolution. The device has an IR touch system with mouse emulation. The monitor is sealed to meet NEMA 4 and 12 (IP65) standards and comes in an aluminum enclosure. The monitor measures 12.72 in. high, 13.47 in. wide, and 5 in. deep. The viewing and touch area is 7.71 in. wide by 5.8 in. high. Operating temperature range is 0 to 45°C. $4180 in volume. **Lucas Control Systems**, Hayward, CA. (510) 471-4700. **Circle No. 381**



Alpha AXP 21064 processor-based computers offer high speed. The MACH 2-245 runs a 233-MHz DEC Alpha AXP 21064 at 245 MHz for a SPECint92 rating of 135 and a SPECfp92 rating of 205. The system costs $7495 to $19,995. The MACH 2-289 runs a 275-MHz Alpha processor at 289 MHz for a SPECint92 rating of 170 and a SPECfp92 rating of 240. The system costs $8495 to $20,995. The computer systems operate as workstations or client/servers for Windows NT, OSF/1, and Unix operating systems. **NekoTech**, Irvine, CA. (714) 580-0055. **Circle No. 382**

Computer keyboard includes audio components for a multimedia station. The Maxi Sound keyboard features two speakers, an omnidirectional microphone, and a master volume-control slide switch. The keyboard includes a universal audio-input jack for other external sound devices or a second microphone. The device has

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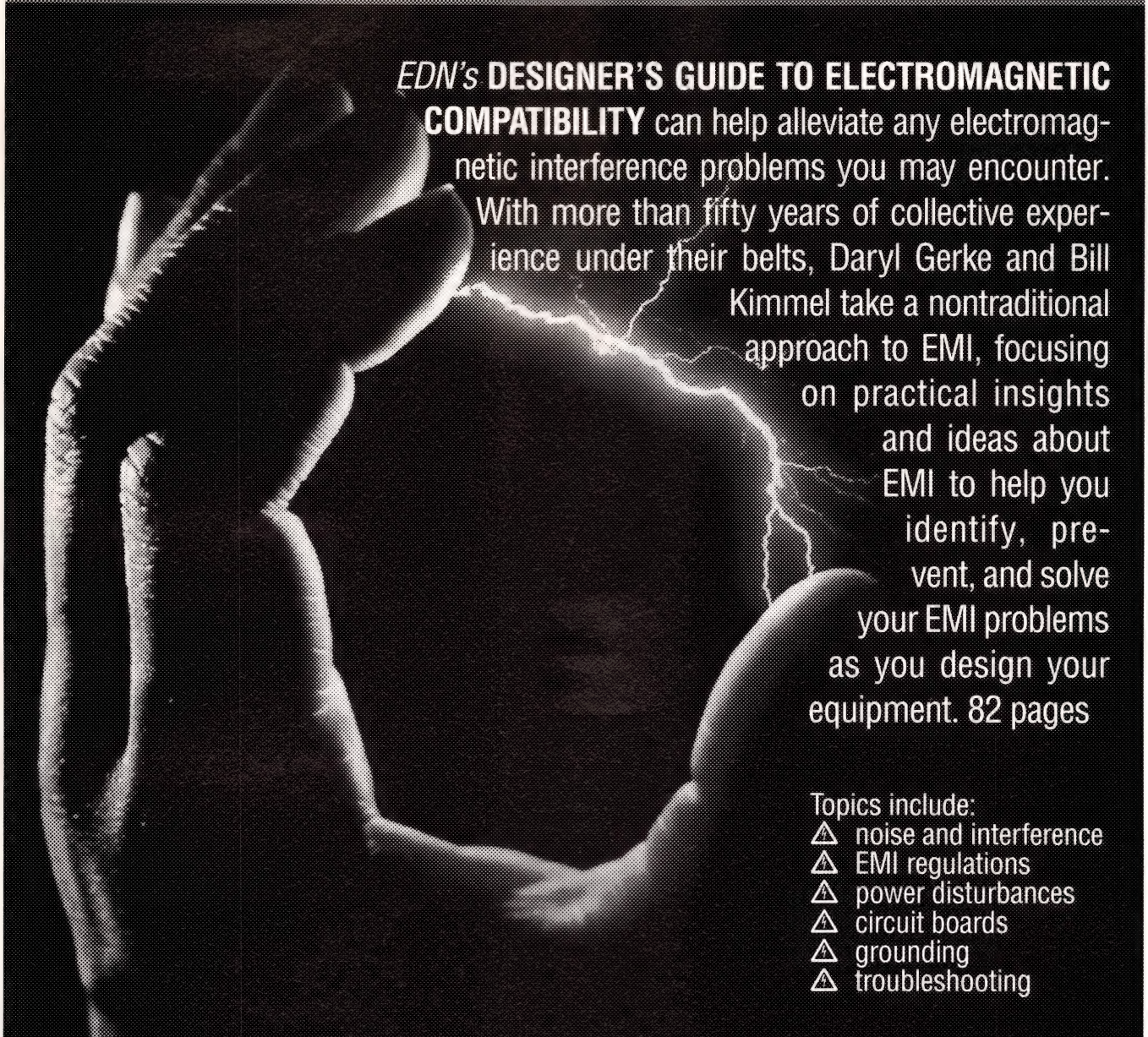

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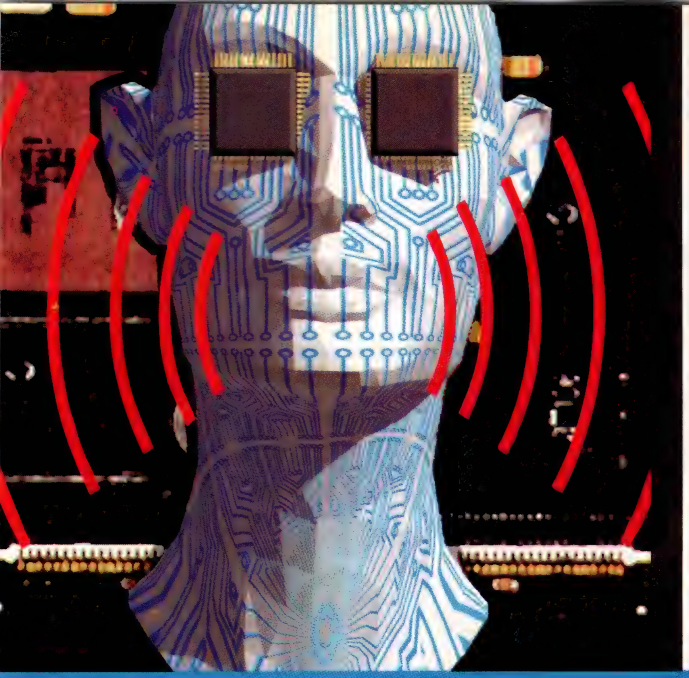

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Design SuperCon '95 is three conferences in one that provides a forum for designers to share information with designers. This super conference focuses on: High-Performance System Design (*EDN*), Digital Communications Design (*EE Times*), and On-Chip System Design (*ASIC & EDA*). The total technical program will feature up to 153 practical design lectures, tutorials, and panels.

Demonstrations That Address Real Design Issues

Demonstrations will illustrate design problems and solutions, many of which will have been presented in conference papers. All of the Design SuperCon '95 exhibitors and speakers invite you to come and interact with them on issues discussed during the presentation and on the demonstration floor.

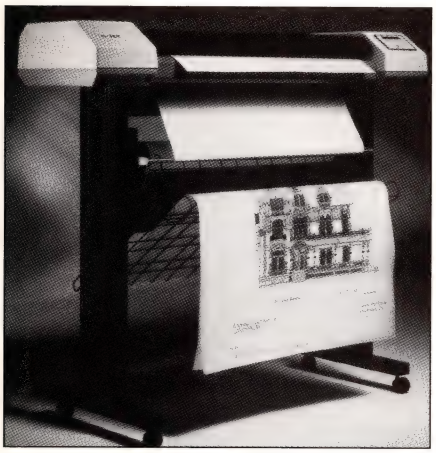
	Digital Communications Design Conference	High-Performance System Design Conference	On-Chip System Design Conference
Conference Themes	Advancing the development of new digital communications products	Providing insights into the development of high-performance computers and embedded-system products	Highlighting recent design experiences with flagship IC products
Practical Design Topics	ATM/B-ISDN: Internetworking Switch Design Transmission Design	Real World Effects High-Speed Data Movement High-Performance Computing Architectures	IC Design Cases New IC Design Methodologies Design Solutions for: • Low-Power and High-Speed Apps. • Design Re-use
Design Experts	Dr. Rafael Gidron, Vice President of Technology, Scorpio Communications Andrew M. Norton, Principal Engineer, Network Equipment Technologies Kenneth B. Finch, Engineering Section Manager, Motorola Computer Group Dr. Praveen Goli, Senior Systems Engineer, TransSwitch Corporation	Nick Tredennick, Ph.D., Chief Scientist, Altera Bill Terrell, Principle Engineer, Vitesse Semiconductor Wayne Fisher, Chairman of PMC Working Group, Director of Stratigic Programs, Force Computers Martin Goetz, Chairman of the JEDEC Committee, ASAT	Scott Baker, Manager, Product Development, Genesis Microchip Lynn Watson, Senior Scientist, Hewlett-Packard Jauher Zaidi, Manager, ASIC Design, Quantum Corporation Mehdy Khatakhotan, Senior ASIC Engineering Manager, S-MOS Systems
Featured Speakers	Joel Birnbaum, Vice President at Hewlett-Packard Labs. Albert Yu, Senior Vice President, Microprocessor Products Group at Intel. Dr. Peter Newman, ATM System Architect at Network Equipment Technologies.		
Participating Companies	AMD, Altera, AT&T, Bellcore, Cadence, Cirrus Logic, Cisco Systems, Digital Equipment Corporation, DSC Communications, Genesis Microchip, Hewlett-Packard, IDT, Intel, LSI Logic, Motorola, Mentor, National Semiconductor, S-MOS, Sun Microsystems, Synopsys, TransSwitch, Viewlogic, VLSI Technology.		
Conference Attendance Fees	Advanced Entrance Fees: $95 for one day • $145 for two days • $195 for all three days On Site Entrance Fees: $115 for one day • $175 for two days • $235 for all three days Conference libraries (three books per conference): $25 per library or $35 on site. There will be two to three Management Workshops per conference. The fee for the workshops is $49. Rooms have been set aside at the Santa Clara Marriott at a discount rate of $99.00 per day during the conference. To receive the discount, mention Design SuperCon when making your reservation. Please call the Marriott directly to make reservations at (408) 988-1500 or 1-800-228-9290 by Feb. 15,1995 to receive the special rate. Rooms are limited; early reservations are required.		

CIRCLE NO. 156

To receive the "Design SuperCon '95 Advance Program," for more information, or to register, call 1-800-772-7842 or (303) 530-4562.

an audio output-jack for a headset, additional speakers, or connection to a stereo system. The keyboard is based on the company's Nova 9200 keyboard and costs $99. **Maxi Switch Inc**, Tucson, AZ. (602) 294-5450. **Circle No. 383**

1024×768 color TFT LCD system offers direct plug-in to standard VGA. The VAMP-XGA can operate directly from standard VGA and SVGA analog signals. A complete package for OEMs includes the 11.8-in. display, all driver electronics, an optional resistive touchscreen, and a 14.5×10.5×3.5-in. metal frame. $7645 (OEM qty). **Computer Dynamics**, Greer, SC. (803) 877-8700. **Circle No. 384**



Monochrome ink-jet printer handles E-size drawings. The Q-Jet 300 produces drawings from 150×150-dpi up to 300×600-dpi resolution. The printer works directly from any CAD software that supports ADI. The QPLOT print-management utility can queue, rotate, resize, nest, and reduce prints. Additional utilities allow conversion of PCX and TIFF files to raster images for the printer. The printer also accepts drawings saved in the HPGL format. Under $5000. **Parallex**, Indialantic, FL. (407) 952-4310. **Circle No. 385**

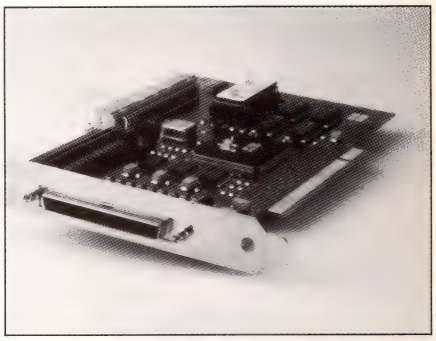
SCSI board for ISA bus offers Plug-and-Play configuration. RT1600E provides automatic configuration and stores the configuration data on EEPROM. The board provides two modes of high-speed data transfers. One mode is in PIO, the other is in DMA. A 128-byte FIFO helps maintain high data-transfer rates. The SCSI board connects up to seven SCSI devices. From $98. **Rancho Technology**, Rancho Cucamonga, CA. (909) 987-3966. **Circle No. 386**

ISA bus SCSI board has automatic Plug-and-Play configuration. The ABP542 uses the Microsoft SCSI Plug-and-Play feature to automatically configure itself when plugged into a computer. The board comes with installation software for computers without the Microsoft Plug-and-Play BIOS. The software automatically configures the board without the need to set switches. The board is able to process 255 simultaneous data requests from an operating system. Internal and external connectors each support seven 10-Mbyte/sec SCSI-2 devices. The board, with Corel's SCSI Version 2 drivers, costs $325. **AdvanSys**, San Jose, CA. (515) 752-5359. **Circle No. 387**

SCSI board for ISA bus costs less than $50. The Fast!SCSI BASIC board is available in an external version ($49.94) and an internal version ($44.95). The board provides economical support for up to seven SCSI devices, including CD-ROM drives, fixed disk drives, tape backup systems, optical drives, and other SCSI devices. The board is capable of SCSI bus transfer rates up to 5 Mbytes/sec and 16-bit PIO transfer rates greater than 3 Mbytes/sec. **QLogic Corp**, Costa Mesa, CA. (714) 438-2200. **Circle No. 388**

16-bit ISA bus SCSI board costs under $100. The BT-540CF SCSI board is 1540-register-set compatible and supports data-transfer rates of 10 Mbytes/sec synchronous and 7 Mbytes/sec asynchronous. Drivers are available for DOS, Windows, NetWare, Windows NT, SCO Unix, OS/2, Solaris, Interactive Unix, UnixWare, and other PC operating systems. The mailbox structure allows 255 simultaneous I/O tasks with minimum host intervention on up to seven SCSI devices. $99 (800). **BusLogic Inc**, Santa Clara, CA. (408) 492-9090. **Circle No. 389**

Touch-input device senses position and pressure. The TouchPad is a low-cost ($20 in volume) device for directing graphics with the touch of a finger. The device uses an array of capacitive lines to detect finger position and pressure. It has no moving parts and uses a combination of neural-based and mixed-signal technology. **Synaptics Inc**, San Jose, CA. (408) 434-0110. **Circle No. 390**



Differential SCSI board for PCI bus offers high performance. The Fast!SCSI IQ PCI-D SCSI board works with cable lengths to 25m and may connect up to 15 SCSI peripherals. The board provides a PCI burst-transfer rate of 132 Mbytes/sec. The device has a SCSI data-transfer rate of 20 Mbytes/sec synchronous and 14 Mbytes/sec asynchronous. $499. **QLogic Corp**, Costa Mesa, CA. (714) 438-2200. **Circle No. 391**

Solid-state disk drives offer up to 950-Mbyte capacity. The ESP5000 family of 5.25-in., solid-state disk drives have capacities to 950 Mbytes. The ESP3000 family of 3.5-in., solid-state disk drives offers up to 268 Mbytes of storage. The storage devices have access times of <100 μsec and a sustained bandwidth of 8 Mbytes/sec for 8-bit transfers and 16 Mbytes/sec for 16-bit transfers. Evaluation units for the solid-state drives are available now. From $7500. **Quantum Corp**, Milpitas, CA. (408) 894-4000. **Circle No. 392**

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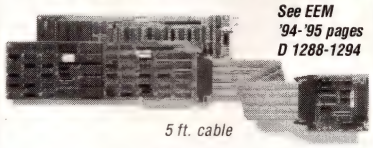

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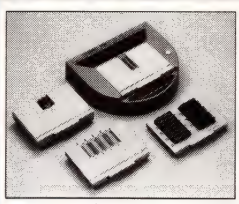

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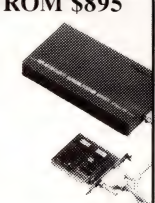

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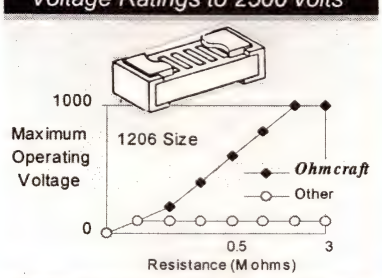

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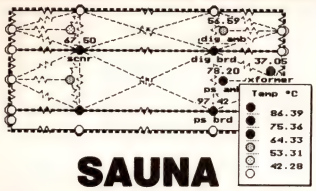

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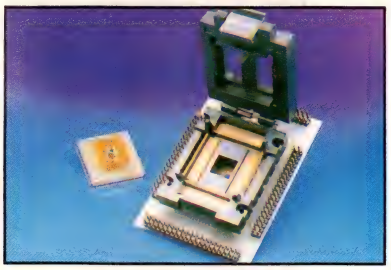

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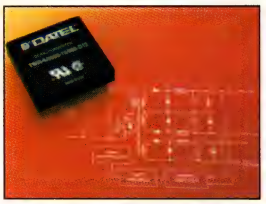

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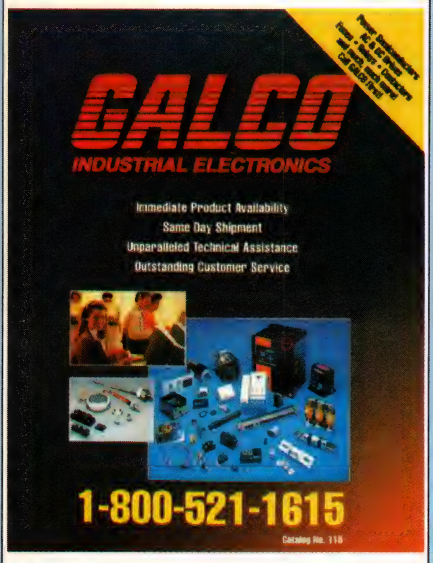

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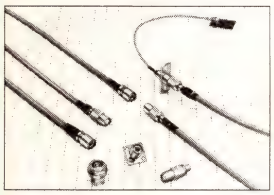

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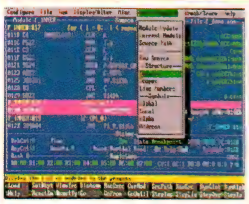

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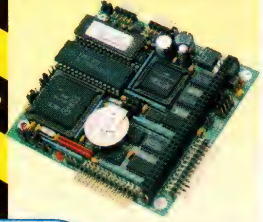

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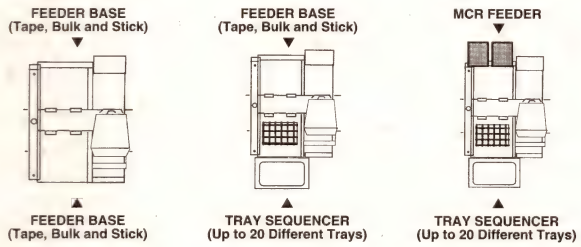

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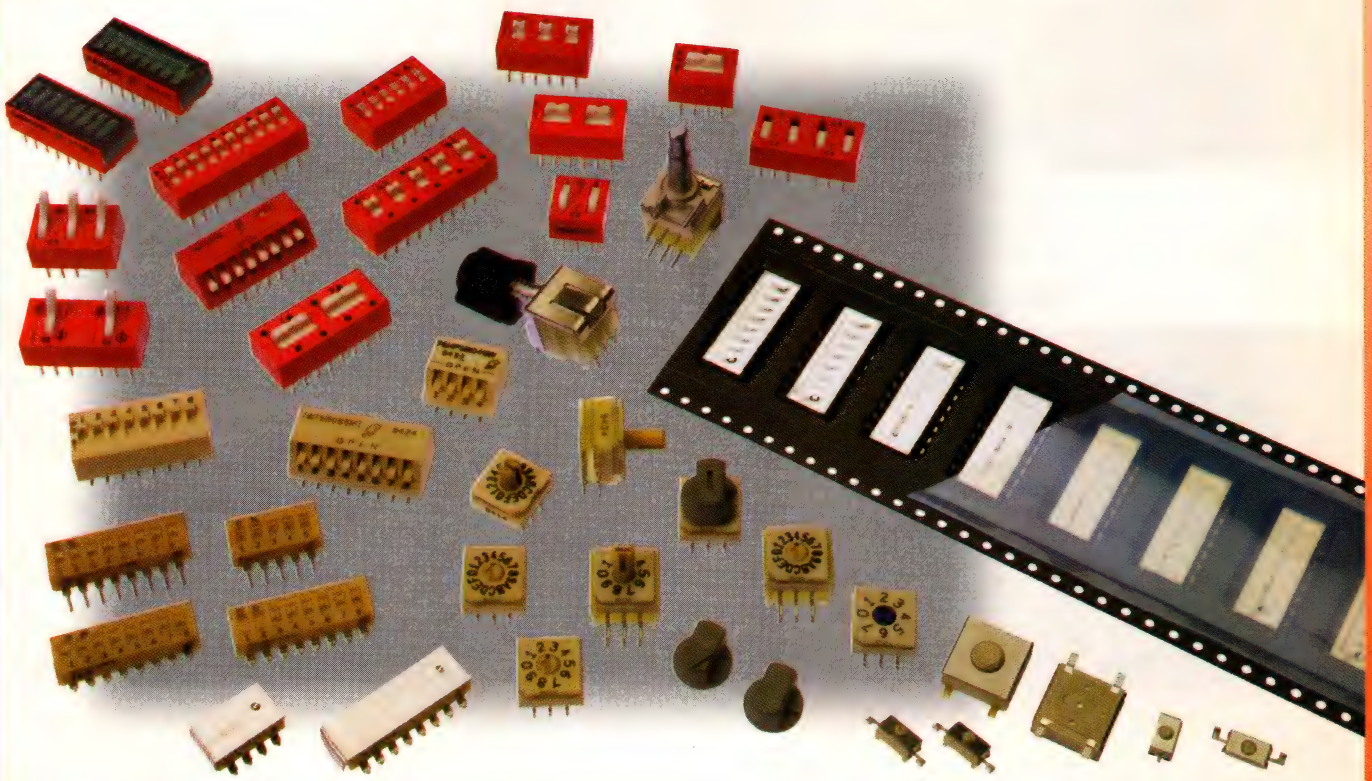

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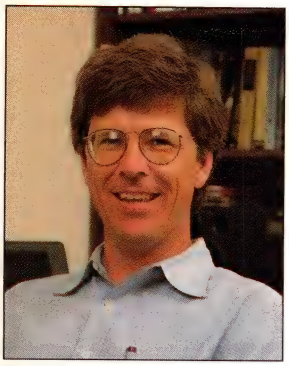

JACK GANSSLE,
EMBEDDED-SYSTEMS
CONTRIBUTING EDITOR

Resistors in digital circuits

When I was a young technician, my associates and I arrogantly believed we could build anything with enough 10k resistors and duct tape. Now it seems that even simple electronic toys use several million transistors encased in tiny SMT packages with hundreds of hairlike leads; no one talks about discrete components anymore.

Yet, no matter how digital our embedded designs get, we cannot avoid certain fundamental electrical properties of our circuits. For example, somehow the digital age has a greater and ever-increasing need for resistors—so many, in fact, that most "discrete" resistors are now usually implemented in a monolithic structure, like a SIP, which is not so different from the ICs they're tied to.

Recently, I dug into a system with a resistor configuration that, although electrically correct, created myriad problems for the user. This configuration is an example of a designer's spending too much time analyzing the best way to use a modern miracle of integration and too little time selecting discrete components because they are, well, boring. No one gets worked up over a lowly carbon resistor anymore; you can no longer buy them piece by piece. At Radio Shack, they come paired in bright decorator packages—for an outrageous sum. Through Digi-Key, the price is right, but you have to buy 100 at a shot.

No matter how digital our embedded designs get, we cannot avoid fundamental properties of our circuits.

The system that got my dander up is reasonably designed. Based on an 8-MHz 80188, memory and I/O are all connected in a carefully thought-out manner. Power and ground distribution are well-planned; noise levels are satisfyingly low. And, yet, the only tool that seemed to work for debugging code was a logic analyzer. Every emulator the poor designer tested failed to run the code properly. Even a ROM emulator gave erratic results.

Though the emulator wouldn't run the user's code, it did show an immediate service of the nonmaskable interrupt (NMI), which wasn't used in the system. Further investigation reveals that the NMI input (which is active high on the 188) was tied low through a 47k resistor.

The system ran fine with a ROM and processor on the board. I suppose the 47k pulldown was at least technically legitimate. A few microamps of leakage current out of the input pin through 47k yield a nice legal logic zero. Yet, this 47k is too much resistance when any sort of tool is installed, due to the inevitable increase in leakage current.

Was the design correct because it violated none of Intel's design specs? I maintain that specs are simply the starting point of good design practice. Never, ever, violate one. And never assume that simply meeting spec is adequate.

A design is correct only if it reliably satisfies all intended applications—including the first of all applications, which is debugging hardware and software. If a design that's technically correct prevents proper debugging, surely you have a problem.

Pulldown resistors are often a source of trouble. It's practically impossible to pull down an LS input (leakage is so high that the resistor value must be frighteningly low). Although CMOS inputs leak very little, be aware of all potential applications of the circuit, including plugging in tools. The solution is to avoid pulldowns wherever possible.

In the case of a critical edge-triggered (read "really noise-sensitive") input like NMI, never pull it low. Tie it to ground. Otherwise, switching noise may be coupled into the input. Even worse, every time you lay out the pc board, the magnitude of the noise problem can change as the tracks move around the board.

Be conservative in your designs, especially when a conservative approach has no down side. If any input must be zero all of the time, simply tie it to ground and never

PHOTOGRAPHY / HOWARD DAVIS

worry about it again. I think designers are so used to adding pullups all over their boards that they design in pulldowns through force of habit.

Once in a while, the logic may indeed need a pulldown to deal with unusual I/O bits. Try to come up with a better design.

Resistor values

Although pulldowns are always problematic, well-designed boards use plenty of pullup resistors. Some are to bias unused inputs, others deal with signals and buses that tristate, and some place switches and other inputs into known one-states.

The biggest problem I see with pullups is using values that are too low. A 100k pullup will bias that CMOS gate properly, but it creates a circuit with a terribly high impedance. Why not switch to 10k? You buy an order-of-magnitude improvement in impedance and noise immunity, yet typically use no additional current, because the gate requires only microamps of bias.

V_{CC} from a decent power supply essentially is a low-impedance connection to ground. Connect a 100k pullup to a CMOS gate, and the input is 100k away from ground, power, and everything else. Overcome a 100k resistance by touching the net with a finger. A 10k resistor will overpower any sort of leakage that humans, humidity, or other effects create.

Besides, that low-impedance connection maintains a proper state no matter what tools you use. In the case of NMI from the example above, the tools weakly pulled NMI high in order that they can run stand-alone (without the target); the 47k resistor was too high a value to overcome this slight amount of bias.

If you are pulling up a signal from off-board, by all means use a very low value of resistance. The pullup can act as a termination as well as a provider of a logic one, but the characteristic impedance of any cable is usually on the order of hundreds of ohms. A 100k pullup is just too high to provide any sort of termination, leaving the input subject to cross coupling and noise from other sources. A 1k resistor helps eliminate transients and crosstalk.

Remember, too, that you may not have a good idea what the capacitance of the wiring and other connections may be. A strong pullup reduces capacitive time constant effects.

Once upon a time, back before CMOS logic was so prevalent, you could often leave unused inputs dangling unconnected and still expect to get a logic one. Engineers are a conservative lot, and most are careful to tie these spare pins to logic-one or -zero conditions.

But what exactly is a logic one? With 74LS logic, it's unwise to use V_{CC} as an input to any gate. Most LS devices happily tolerate up to 7V on V_{CC} before something fails; the input pins have an absolute maximum rating of approximately 5.5V. Connecting an input to V_{CC} creates a circuit where small power glitches the devices can tolerate may blow input transistors. It's far better to connect the input to V_{CC} through a resistor, thereby limiting input current and yielding a more power-tolerant design.

Once upon a time, back before CMOS logic was so prevalent, you could often leave unused inputs dangling unconnected and still expect to get a logic one.

In most of its guises, modern CMOS logic has the same absolute maximum rating for V_{CC} as for the inputs, so it's perfectly reasonable to connect input pins directly to V_{CC} if you're sure that production will never substitute an LS equivalent for the device you've called out.

CMOS does require that every unused input be pulled to a valid logic zero or one to avoid generating an SCR latch-up condition.

Fast CMOS logic (like 74FCT) switches so quickly that, even at very low clock rates, glitches with Fourier components into billions of cycles per second are not uncommon. Reduce noise susceptibility by tying your logic zeros and ones directly to the power and ground planes. Avoid pullups and pulldowns, for they increase parts counts and reduce reliability.

Yet, one must balance the rules of good design with practical ways to design a debuggable system. A thousand years ago, circuits used vacuum tubes mounted on a metal chassis. All connections were made by point-to-point wiring; thus, making engineering changes during prototype check-out must have been fairly easy. Later, transistors and ICs lived on pc boards, but incorporating modifications was still pretty simple. Now, we're faced with whisker-thin leads on surface-mount components, with 8- and 10-layer boards where most tracks are buried under layers of epoxy and out of reach of X-Acto knives. If we tie every unused input (even on our spare gates) to a solid power or ground connection, it's awfully hard to cut the connection free to tie it somewhere else. Lifting the pins on those spare gates might be a nightmare.

It seems the solution is to build the prototype boards a bit differently from the production versions. I look at a design and try to identify areas most likely to require cutting and pasting during check-out. A prime example is a programmable device, a PAL or an FPGA. Experience has taught me that probably I'll forget a crucial input to that PAL, or that I'll need to generate some nastily complex waveform using a spare output on the FPGA.

Embarrassing situation

Some engineers figure if they socket the programmable logic, they can lift pins and tack wires to the dangling input or output. I hate this solution. It sometimes takes an embarrassing number of tries to get a complex PAL right; each time you must remove the device, bend the leads back to program it, and then reinstall the mods. (An alternative is to put a socket in the socket, and lift the upper socket's leads.) When the device is a PLCC or other non-DIP, it's even harder to get access to the pins.

I leave all unused inputs on these devices unconnected when building the prototype, which, unfortunately,

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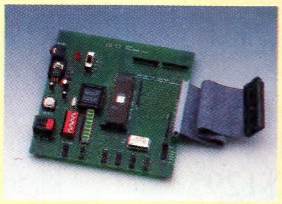

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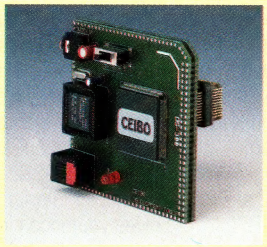

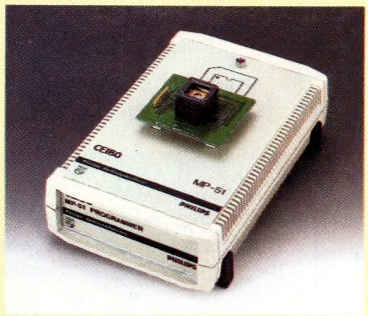

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creates a window of vulnerability to SCR latch-up conditions. Then, it's easy to connect mod wires to the unconnected pins. When the first prototype is done, I change the schematic to properly tie off the unused inputs, so prototype No. 2 (the production units) is designed correctly.

In years of doing this, I have never suffered a problem from SCR latch-up due to dangling pins. The risk is always lurking, waiting for an unusual ESD—or perhaps even a careless, ungrounded finger biasing an input.

I tie spare gate inputs to ground, even with the first run of boards. It just feels a little too dangerous to leave an unconnected 74HC74 lead dangling. However, if at all possible, I have the person doing the pc-board layout connect these grounds on the bottom layer so that a few quick strokes of the X-Acto knife can free them to solve another last-minute "whoops."

This scenario brings up another important point, which is that the days of wire-wrap prototypes are dead. Modern logic is simply too fast to support anything but the best quality multilayer pc boards (with solid ground and power planes) even during prototyping. It's cheap to get two copies of a prototype pc board built quickly; just search through the little ads in the back of this magazine for sources of quick-turn boards. By planning for disposable prototype pc boards, you can eliminate all sources of untraceable weirdness from a noisy prototype and can easily make small changes to the design just for the sake of increasing the product's debuggability.

In designs that use through-hole parts, leave just a bit of extra room around each chip so you can socket the parts on the prototype. It's a lot easier to pull a connected pin from a socket than to cut it free from the board.

Here are a few concluding thoughts:

- Avoid pulldown resistors at all costs!
- Don't be afraid to use low resistor values, even in CMOS circuits. A static pullup needs only microamps, no matter what resistor value you select.
- Because we spend far more time troubleshooting our designs than actually drawing schematics, lay out the prototypes in an easy-to-debug form. You can change them in production.

Jack Ganssle is the president of Soft-aid, a vendor of emulators and other embedded-systems tools. He can be contacted via Compuserve at "76366,3333," or via Internet at "jack@softaid.com." For those users of the Pony Express send mail c/o Soft-aid, 8310 Guilford Rd, Columbia, MD 21046.

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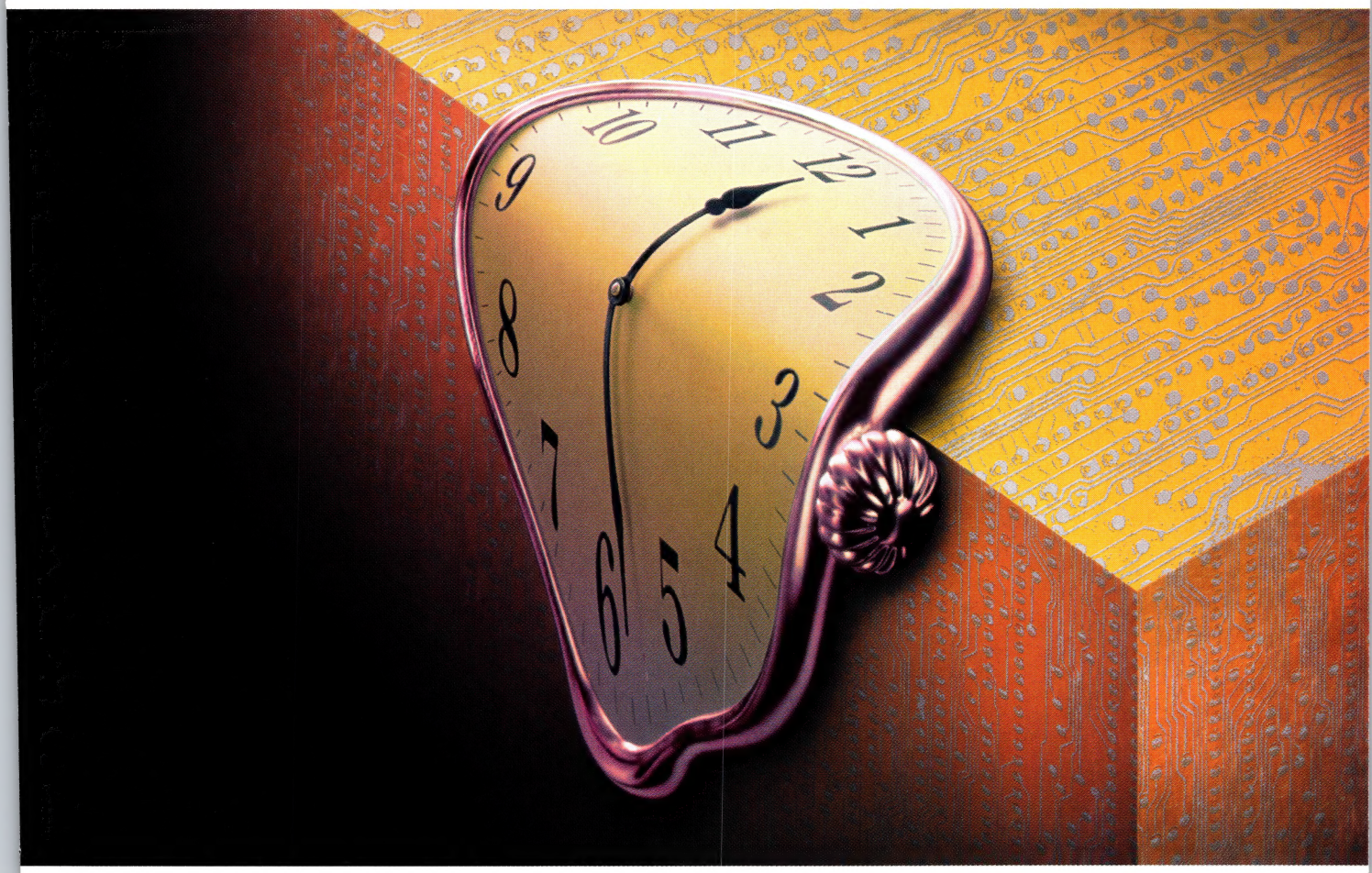

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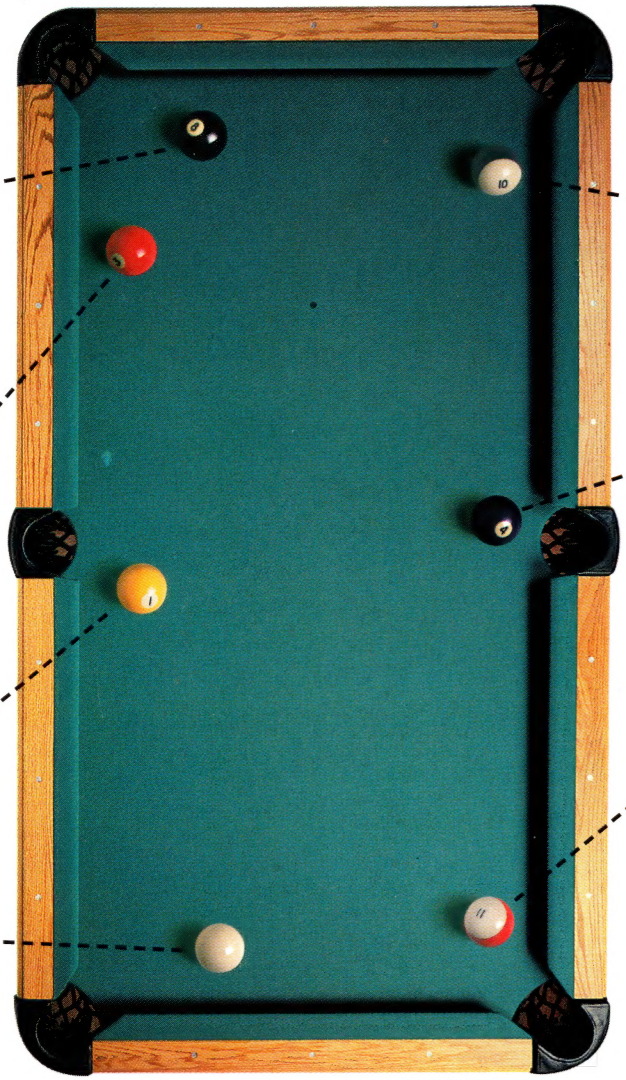

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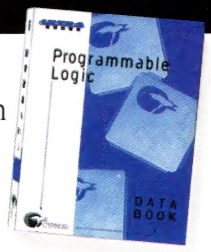

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